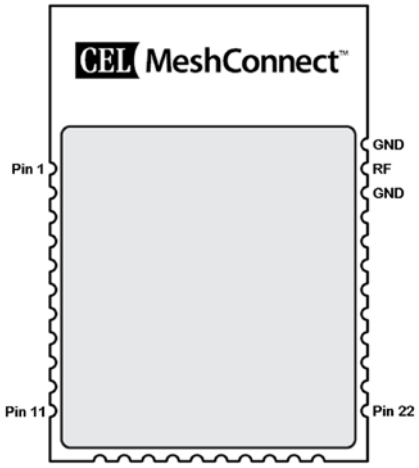
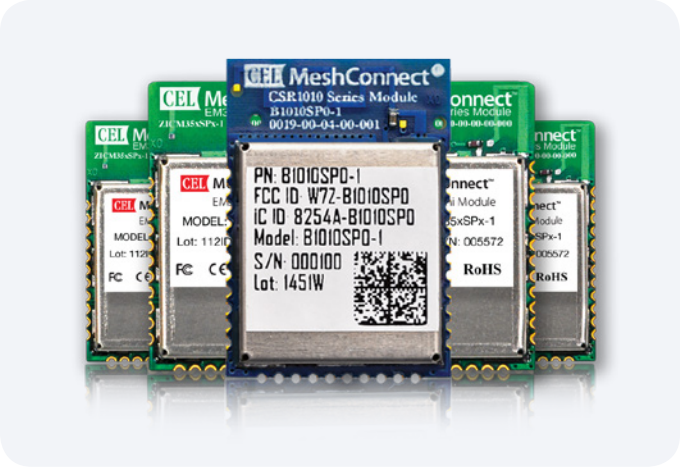
Mini Modules Castellation Pin Layout Guidelines - For External Antenna

Dcoument No:
0011-00-17-03-000 (Issue C)





INTRODUCTION

The ZigBee/Thread EM35x (ZICM357SP0-1C, ZICM357SP2-1C, ZICM357SP2-2C, ZICM3588SP0-1C, ZICM3588SP2-1C, and ZICM3588SP2-2C) and Bluetooth Smart CSR1010 Mini Modules (B1010SP0-1C-R) from California Eastern Laboratories (CEL) provide an optional RF port castallation pin for using an external antenna. This User Guide details the layout guidelines of the RF port castellation pin to achieve optimum antenna performance.

Layout Guidelines for using Mini Module RF Castellation Pin

Mini Modules that include the letter "C" near the end of the part number designate connectorized. Connectorized Mini Modules have the RF output routed to castellation pin 32 (instead of the trace antenna) so that an external antenna may be used. This User Guide will assist customers to properly match the impedence to provide a 50 Ω termination to the RF castellation pin. Under these conditions, the CEL FCC Certification for the module trace antenna does not apply and the end user is responsible for complying with regulatory requirements.

In order to provide as much flexibility as possible for the various host boards that could be used, the RF signal is routed to castellation pin 32, with castellation pins 31 and 33 connected to ground. This configuration provides the option of using either a coplanar waveguide transmission line layout or microstrip transmission line layout. The better option to use depends on the host Printed Circuit Board (PCB) construction. For a two-layer design, the coplanar waveguide will likely be the preferred choice, whereas for multi-layer designs, the microstrip will likely be the preferred choice.

There are many different tools that can be used to determine the transmission line structure. Typically, the tools allow you to enter the parameters of your PCB, such as dielectric constant, dielectric thickness between the RF trace and the RF ground plane and the copper thickness used for the transmission line. CEL used Agilent's LineCalc software tool to calculate the transmission line structures for both a coplanar waveguide with ground structure and the microstrip transmission line. Each will be described in this User Guide.

Coplanar Waveguide

The coplanar with ground plane waveguide structure is made up of the RF trace on the topside of the PCB with adjacent ground planes spaced close to the RF transmission line. A ground plane under the RF trace may also exist and may influence the transmission line properties depending on the thickness of the dielectric.

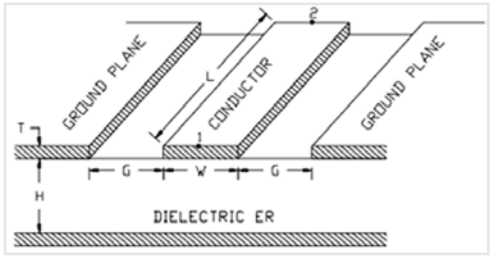


Figure 1. Coplanar Waveguide

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Agilent's LineCalc contains a model for this type of structure and allows the user to easily enter the PCB parameters to simulate the transmission line width and gap which will yield a 50Ω transmission line. Alternatively, if using a specific transmission line width, then the width and gap can be entered into LineCalc and analyzed to determine the resulting impedance. Using the second approach, and presuming a typical two-layer 62 mil thick FR4 PCB will be used for the host board, the parameters in Figure 2 were entered into LineCalc:

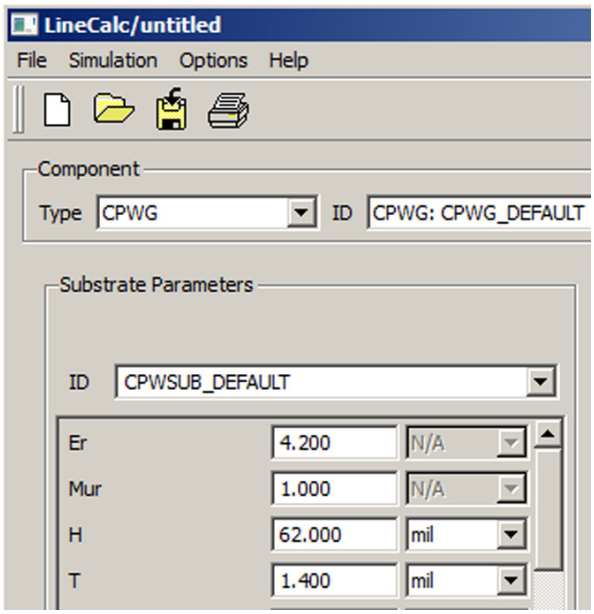

Figure 2. LineCalc Parameters

Since the module castellation is 40 mils wide on the bottom of the module, an RF trace width of 40 mils is entered into the physical properties along with a gap of 8 mils separation from the ground plane. Using a transmission line width equal to the castellation pad width eliminates any RF discontinuity which could degrade the return loss. Selecting the "Analyze" button yields an RF impedance of 51.5Ω. This calculates a return loss of better than -36dB.

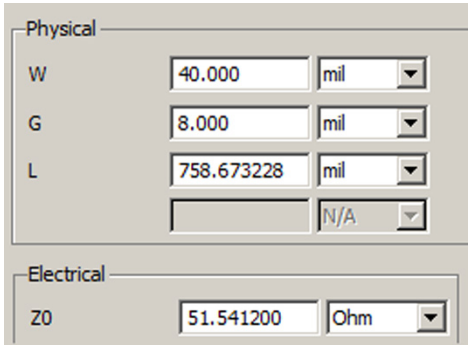

Figure 3. RF Properties

An example of the layout is shown in Figure 4. Red represents the top layer and green represents the bottom layer of the two layer design.

Note: *There should be a continuous ground plane on Layer 2 under the RF trace.*

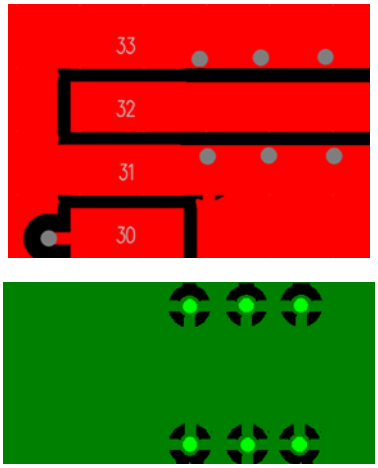

Figure 4. Layout Example *(Top)*
RF Bottom Layer *(Bottom)*

Microstrip Transmission Line

The microstrip structure is typically used when the width to height ratio of the transmission line to the ground plane is between 1 and 10, which often happens when a multi-layer PCB is used.

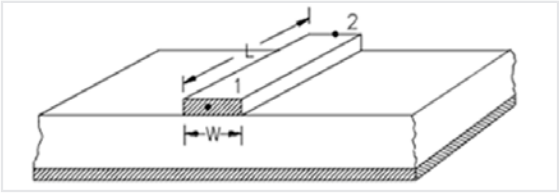

Figure 5. Microstrip Structure

For a four-layer board, presuming the top dielectric thickness specified is 20 mils thick between Layer 1 (RF layer) and Layer 2 (ground plane), the overall thickness of the PCB would be about 64 mils when taking the thickness of the copper into account. Again, using the LineCalc tool and entering the PCB parameters for both the desired transmission line width and the dielectric material parameters, the calculated impedance for a 40 mil wide transmission line is 48.6Ω. This is a return loss of better than -36dB. The relevant LineCalc simulations are shown below in Figure 6.

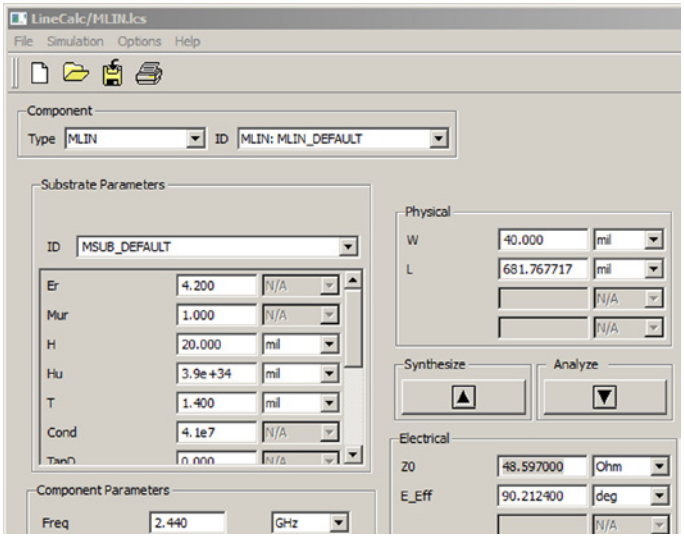

Figure 6. LineCalc Simulation Parameters

The artwork that implements the microstrip for Layers 1 and 2 is shown in Figure 7. Notice that there is no ground plane along the RF trace. If a ground plane is desired, a minimum gap of 1.5 times the RF trace width should be used so that the structure does not approach the coplanar waveguide structure and impact the realized impedance.

Again, a continuous ground plane is required under the microstrip line on Layer 2 to implement the RF microstrip structure. One of the advantages of the microstrip implementation is that the remaining layers under Layer 2 are available for routing signals. See Figure 8 for an example of the RF ground plane with ground vias.

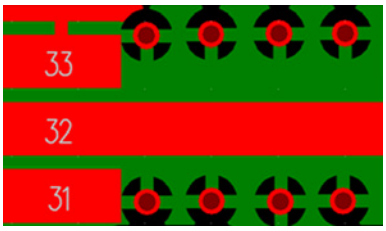

Figure 7. Microstrip artwork for Layers 1 and 2

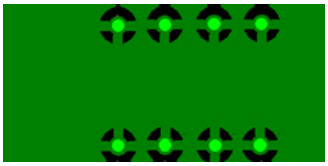

Figure 8. RF ground plane with ground vias

CEL Coplanar Layout Example

The following example implements the coplanar waveguide approach, with a two-layer 62 mil thick FR4 PCB. The measured return loss is -23 dB at 2.44 GHz using this approach. The difference between the measured -23 dB and the predicted -36 dB return loss could be due to etching tolerances, differences in dielectric constant or even PCB thickness. A return loss of -23 dB equates to a transmission loss of power of 0.08 dB which is acceptable. A plot of the measured impedance of the example layout is shown in Figure 9.

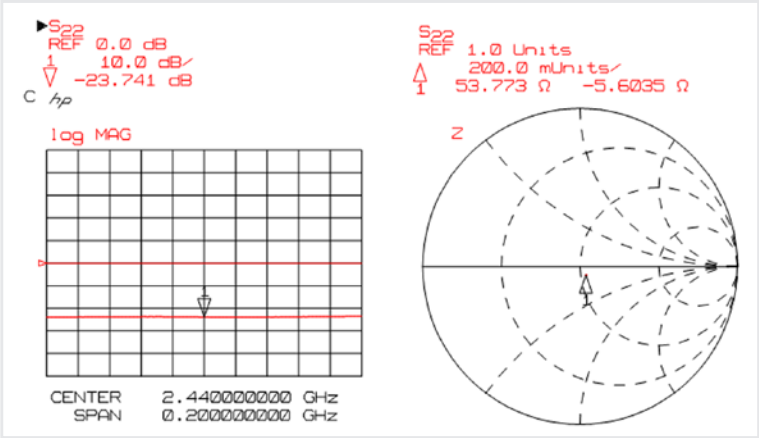

Figure 9. Daughtercard Impedence

The table in Figure 10 illustrates how the variations in the dielectric constant and dielectric thickness influence the transmission line characteristic impedance. It also shows that the coplanar waveguide transmission line is preferable with thicker dielectric materials since the transmission line trace width is closest to the castellation thickness.

Coplanar Waveguide with Ground

Material	Er	T (mils)	H (mils)	Width (mils)	Gap (mils)	Zo (Ω)
FR4	4.2	1.4	62	40	8	51.5
Getek	3.9	1.4	62	40	8	53.1
FR4	4.2	1.4	62	40	6	47.5
Getek	3.9	1.4	62	40	6	48.9

Microstrip

FR4	4.2	1.4	31	60	-	49.9
Getek	3.9	1.4	31	60	-	51.5
FR4	4.2	1.4	20	40	-	48.6
Getek	3.9	1.4	20	40	-	50.2
FR4	4.2	1.4	10	18	-	50.8
Getek	3.9	1.4	10	18	-	52.5

Figure 10. Impedance Characteristics

Antenna Matching Considerations

Routing the RF signal to a castellation point provides customers maximum design flexibility when using their own antenna with the Mini Modules. Many antennas require RF matching to achieve the specified performance. Therefore, some customers may consider adding at least a series and a shunt matching component. If additional board space is available, adding three matching components (in a series - shunt - series configuration) will provide a broader impedance match. The specific type of component (inductor or capacitor) and its value would be unique to the chosen antenna and the impedance that must be matched. However, using a series inductor and a shunt capacitor implements a low pass matching network and will provide some attenuation of the higher order harmonics. The schematic illustrating the series - shunt - series configuration is shown in Figure 11 where the termination on the left represents the castellation pin (or 50Ω load) to which the antenna is matched.

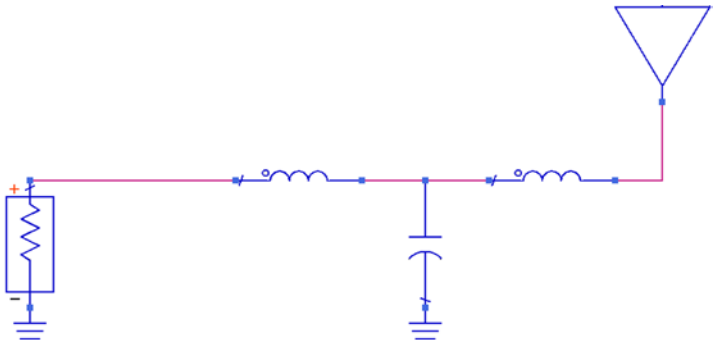

Figure 11. Antenna Matching Circuit

CONCLUSION

This User Guide provided general guidelines for the RF interface to the CEL Mini Modules for those users who wish to use the castellation pin. Two primary PCB structures were considered: a double sided FR4 host board and a multilayer board. Using Agilent's LineCalc software tool, examples were provided that detailed how to realize a 50Ω transmission line on their host board. Also included was the addition of matching components that might be placed on the host board to allow for RF impedance matching to a specific antenna. The value of additional components is determined by the specific antenna impedance and the type of matching topology chosen.

REFERENCES

Reference Documents	Download
California Eastern Laboratories	
0011-00-07-00-000 -MeshConnect EM35x Mini Modules Datasheet	Link
0019-00-07-00-000 -MeshConnect B1010SPx Mini Modules Datasheet	Link

REVISION HISTORY

Previous Versions	Changes to Current Version	Page(s)
0011-00-17-03-000 (Issue A) September 6, 2012	Initial Release	N/A
0011-00-17-03-000 (Issue B) June 10, 2013	Format update	All
0011-00-17-03-000 (Issue C) September 18, 2015	Added New ZigBee/Thread and Bluetooth Smart Mini Modules	All

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