The development of this amplifier includes the modeling and the characterization of the “twin” gallium-arsenide metal-semiconductor-field-effect-transistor (GaAs MESFET) device, NES2427P-60 used in this design. This article also presents the design methodology of the external input- and output-matching circuits of the GaAs device and a two-arm branch 90-deg. coupler. The performance of this compact amplifier is presented and discussed.

The goal was to design a compact linear PA using the 60-W Class A-B NES2427P-60 from NEC/CEL that delivers a power of +40 dBm for each tone with an IMD3 of less than -40 dBc over the 2.5-to-2.7-GHz S-band instantaneous bandwidth. The requirement for the typical gain at 1-dB compression (P1dB) was 11 dB with a gain flatness of better than ±0.5 dB. The target for the typical output power at P1dB was +48 dBm.

The amplifier-circuit optimization for linearity and the accurate prediction of the amplifier’s performance require an available device model and characterization for a two-tone signal. The device was modeled and characterized with a two-tone signal at an output-power level of +40 dBm.
The design challenge was to match the device’s optimum output impedance for IMD3 to a 50-Ω load over the 2.5-to-2.7-GHz bandwidth with an excellent return loss (better than 18 dB) and to minimize the loss of the output matching and combining circuit. The input circuit is not as critical as the output since it does not significantly affect the output power of the amplifier. Its matching and loss must be excellent only at the maximum frequency for gain consideration. Stability is always an issue with high-power amplifiers. The splitter and combiner have to be selected for high isolation (20 dB), low loss (0.25 dB), good balance, and ease of integration to the amplifier layout. The choice of the amplifier configuration is important if a good external match is needed to isolate the driver from the power stage.

A MESFET MODEL

The device used in this amplifier (a Class A-B MESFET “twin” device) consists of two separated pairs of chips with their internal matching circuits mounted in the same package. The package has two gate connections and two drain connections without any internal connections between the two sides of the device to take advantage of the virtual ground created by the push-pull configuration. The high-power GaAs devices at L-band and higher frequencies do not have these internal connections because their transverse dimensions are too large. Therefore, these devices are not “push-pull.” They are devices with two identical sides called (by CEL) “twin” devices. The configuration of the amplifier defines only how the devices operate. They can be combined the same way as single-ended parts in balanced configuration (90-deg. hybrid), in push-pull configuration (baluns), and in phase combining (Wilkinson), etc.

To model these devices, only one side is considered. Simple narrow-band external input- and output-matching circuits with biasing circuits were designed. At each frequency, the input circuit was tuned for maximum return loss and between the two sides of the device. These devices are sometimes improperly called “push-pull” devices. This concept comes from lower-frequency applications—high frequency (HF), very-high frequency (VHF), and ultra-high-frequency (UHF)—using silicon (Si) devices with internal connections between the two sides of the device to take advantage of the virtual ground created by the push-pull configuration. The high-power GaAs devices at L-band and higher frequencies do not have these internal connections because their transverse dimensions are too large. Therefore, these devices are not “push-pull.” They are devices with two identical sides called (by CEL) “twin” devices. The configuration of the amplifier defines only how the devices operate. They can be combined the same way as single-ended parts in balanced configuration (90-deg. hybrid), in push-pull configuration (baluns), and in phase combining (Wilkinson), etc.

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the output circuit was optimized for IMD3. The performance, the source, and the load impedances were measured and recorded. These impedances are relatively high and do not present any difficulty in measuring to good accuracy because the device is internally prematched.

Table 1 shows the half-device impedances versus frequency. Under these conditions and for half the device, the following performance was obtained in the 2.5-to-2.7-GHz band—P1dB = +45 dBm, IMD3 = -41 dBc to -43 dBc at +37 dBm each tone, and G1dB = 13.3 dB.

5. This set of curves shows the relationship between Pout, Pin, Ids, and Pin for the amplifier. The measurements were made at three different frequencies for each set (2.5, 2.6, and 2.7 GHz).
In addition to the device characterization with a two-tone signal, the device was characterized with one-tone signal at P1dB and its S-parameters were measured under small-signal conditions in the 1.5-to-3.5-GHz band. The S-parameters were used for gain and stability analysis under small-signal conditions.

Contrary to popular belief, for a bandwidth of less than one octave there are no advantages in using a push-pull amplifier in terms of bandwidth and linearity. The disadvantages are:

1. Low isolation between the two sides of the device if a classical balun is used (only 6 dB).
2. Poor external input and output match.

On the other hand, the balanced configuration has the same perfor-

6. IMD3 as a function of P_{out} is shown here for various values of I_{dsq} over the 2.5-to-2.7-GHz range. The best IMD3 performance is achieved at the highest level of I_{dsq}, 12 A.

7. These curves are similar to those of Fig. 6, except that IMD5 is plotted against power. And like Fig. 6, IMD performance improves for higher values of I_{dsq}.
MMDS Amplifier

Table 2: Comparison of simulated and measured impedances

<table>
<thead>
<tr>
<th>Frequency GHz</th>
<th>Source impedance of half NES2427P-60</th>
<th>Load impedance of half NES2427P-60</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Measured</td>
</tr>
<tr>
<td>2.4</td>
<td>6.2 + j4.8</td>
<td>5.0 + j7.4</td>
</tr>
<tr>
<td>2.5</td>
<td>7.1 + j4.9</td>
<td>7.5 + j7.1</td>
</tr>
<tr>
<td>2.6</td>
<td>7.4 + j3.6</td>
<td>8.0 + j4.0</td>
</tr>
<tr>
<td>2.7</td>
<td>4.9 + j2.3</td>
<td>4.6 + j2.8</td>
</tr>
</tbody>
</table>

Performance as the push-pull concerning bandwidth and linearity (bandwidth less than one octave) and has the following advantages:

• High isolation between the two sides of the device.
• Good external match.
• Easy-to-design printed 90-deg. splitters/combiners for narrowband applications that can be easily integrated with the layout of the amplifier.
• Good reliability—the failure of one device side does not result in total failure. Only the output power drops by 6 dB.

For balanced amplifiers, many kinds of couplers that can be used—Lange couplers, Wilkenson with 90-deg. phase jog on one port, two-arm branch 90-deg. hybrid, etc. In this project, a two-arm branch 90-deg. hybrid was selected due to its simple layout and ease in integrating with the amplifier layout. Since the input- and output-matching circuits realize the matching of the device to 50-Ω impedance, the hybrid does not perform any impedance transformation and all its port impedances are 50 Ω.

The design of the hybrid was performed with Hewlett-Packard (now Agilent) HP multipoint-distribution software (MDS). Also, HP MOMENTUM software was used to perform the electromagnetic (EM) simulation. The comparison of the simulated results between MDS and MOMENTUM software showed a slight difference in the coupler layout. The final EM simulation indicates that this 90-

8. The curves of IMD7 with respect to $P_{out}$ follow the same pattern as those of Figs. 6 and 7, showing how IMD performance improves for higher values of drain current.
deg. hybrid has more than 20 dB of isolation between its coupled ports and 20 dB of return loss for each port. Its balance is better than 0.1 dB in magnitude and 90 ± 1 deg. in phase.

The input-matching circuit was optimized for flat gain over the 2.4-to-2.7-GHz bandwidth and to provide the best match to a 50-Ω impedance at the highest frequency. It consists of two sections using only transmission lines with all stubs being open. In order to cover the 2.4-to-2.7-GHz bandwidth, sections with low quality factor (Q) were selected for the design, especially the first one. A gain slope of −6.0 dB per octave for the device was assumed and the input-matching circuit was designed to compensate for this slope and to obtain an excellent match at 2.7 GHz. The result is a flat gain and a maximum gain over the desired bandwidth. From the device modeling and characterization data the predicted associated gain was $G_{1dB} = 13.0$ dB and the gain flatness was 0.5 dB. The simulation also showed an input-return loss of more than 12 dB across the bandwidth for half the device. However, the full device return loss will be higher since a balanced configuration was selected and the two device sides are symmetric.

The design goal for the output matching network was to present the optimal load impedance for a two-tone signal at a defined output power with minimum loss. Since the NES2427P-60's device-output optimal impedance for a two-tone signal is not far from 50-Ω impedance, two sections of one-sixteenth wavelength Chebyshev impedance transformer circuit was selected. This circuit minimizes the dimensions and loss of the matching network. The simulation showed that the loss of this output circuit was less than 0.2 dB and the return loss was better than 19 dB across the bandwidth.

Figure 1 shows the complete balanced-amplifier layout. The two-arm branch 90-deg. hybrid, which uses the same substrate as the matching circuit, is integrated with the amplifier layout and does not require any additional connection. All the circuits are directly printed on the same $\varepsilon_r = 2.2$.
(continued from p. 61)

31-mil-thick substrate. Standard 50-Ω loads are connected to the coupler-isolated ports. The amplifier is compact and easy to assemble. The total dimensions of the amplifier are 13.2 × 6.0 cm².

**TEST RESULTS**

The source and load impedances presented by the circuit to the device directly from simulation were measured versus frequency with a vector network analyzer (VNA). The experimental results showed good agreement between the measured and simulated impedances (Table 2). However, a slight tuning was performed with the use of a VNA on the input- and output-matching circuits to obtain the exact simulated impedance values.

The amplifier was tested in a 50-Ω system with fixed broadband tuning corresponding to an optimum IMD3 performance in CEL’s high-power automated setup. The device was biased at $V_{ds} = +10$ VDC and $I_{dsq} = 12$ A. Figure 2 shows the $P_{1dB}$ and $G_{1dB}$ performance versus frequency. Figure 3 provides power-added efficiency (PAE) and $I_{ds}$ versus frequency at 1-dB gain compression. It shows that the amplifier exhibits a typical PAE of 40 percent from 2.4 to 2.7 GHz.

Figure 4 shows the IMD performance of the amplifier. The curves show that the amplifier has good IMD performance with an IMD3 lower than $-42$ dBc at +40-dBm output power, each tone across the 2.5-to-2.7-GHz MMDS bandwidth. $P_{out}$ and $I_{ds}$ versus $P_{in}$ and frequency are shown in Fig. 5.

The amplifier-input return loss over the 2.5-to-2.7-GHz bandwidth was better than 15 dB, which is better than the expected return loss for a push-pull configuration. The amplifier’s IMD performance was measured with fixed tuning at a constant, $V_{ds} = +10$ VDC, and at constant frequency of 2.7 GHz, versus $P_{in}$ and $I_{dsq}$. Figures 6, 7, and 8 show respectively IMD3, IMD5, and IMD7. The curves show, as expected, that this amplifier exhibits the best IMD3 performance at any $P_{out}$ level when biased at the highest $I_{dsq}$, 12 A. The maximum $I_{dsq}$ is limited only at $V_{ds} = +10$ VDC by the maximum recommended channel temperature which is 150°C.

The mean time to failure (MTTF) of GaAs power devices is limited by their channel temperature. It is important for amplifier designers to be able to calculate this temperature for their applications from the device power dissipated, the case temperature, and its thermal resistance ($R_{th}$). This calculation is not as simple as it may appear since the $R_{th}$ of GaAs devices is a strong function of the device-flange temperature and the channel temperature, or the power dissipated. The NE S2427P-60 data sheet and CEL’s application note5 AN1032 give the information necessary to calculate $R_{th}$ versus the flange and channel temperatures, or power dissipated.

The NE S2427P-60 data sheet indicates $R_{th} = 0.76K/W$ maximum for $T_f = 25°C, V_{ds} = +10$ VDC, $I_{ds} = 12$ A and recommends a maximum channel temperature of 150°C. This temperature corresponds to a MTTF of $2.4 × 10^6$ h. From these data and with the help of the application note, the maximum $I_{dsq}$ can be calculated versus the device-flange temperature.

As an example, for a maximum flange temperature of 52°C, the maximum power dissipated corresponding to a channel temperature of 150°C is $P_{diss.} = 120$ W. It means the maximum quiescent $I_{dsq}$ for $V_{ds} = +10$ VDC and a flange temperature of 52°C is 12 A. This current is relatively high, but it is lower than half of the device-saturated drain current ($I_{dsq}$) which is 36 A typical. If the standard definition of class A for power devices is used, $I_{dsq} = 12$ A does not correspond to this device for a Class A operation but to a Class A-B one.

**References**

1. NES2427P-60 data sheet, http://www.cel.com