To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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Technical Note

Optical/Microwave Semiconductor Devices

Review of Quality and Reliability Handbook
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PREFACE

Thank you very much for using optical and microwave semiconductor products manufactured by NEC Electronics Corporation Compound Semiconductor Devices Division.

This Optical and Microwave Semiconductors Quality/Reliability Handbook describes policies on and activities for quality and reliability assurance that are reflected in our products, as well as evaluation and analysis technologies.

Compound Semiconductor Devices Division provides “best mix solutions” composed of cutting-edge optical technologies as well as silicon and compound semiconductor microwave technologies that open up new possibilities for users.

In order to provide the best mix solutions, we recognize that high product quality and reliability are of paramount importance, and have been working in concerted fashion to improve our operations at every stage from design and development to manufacturing and logistics. This manual, which is designed to help users understand the quality and reliability assurance applied to our products so that they can make the most of our products' quality and reliability and contribute to their activities, and as such, it should be used in conjunction with other relevant documents.

In the future, Compound Semiconductor Devices Division will continue to serve our customers as a business partner seeking ever better quality improvements and innovations, and we thereby hope to ensure the highest possible levels of customer satisfaction. Advice and guidance from the users are truly appreciated.

June 2006

NEC Electronics Corporation Compound Semiconductor Devices Division
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CHAPTER 1 QUALITY ASSURANCE SYSTEM

1.1 Quality System

(1) Basic policy (company doctrine)
One of the advantages that Compound Semiconductor Devices Division has is that we can provide optimum solutions faster than other companies. Our broad network is composed of in-house divisions and related companies that engage in various processes such as research, development, and production. This means our company can bring together and utilize various expertise and technologies. All product development programs are integrated into a single R&D&P (Research & Development & Production) system to realize greater efficiency. Technical issues brought to us by our customers are channeled directly to our R&D Group, which helps to ensure a smooth transition to mass-production once the development stage is completed. Thanks to this comprehensive collaboration system, we are able to promptly serve our customers' needs. Backed by our cutting-edge technologies, an R&D&P system, and detailed technical support, Compound Semiconductor Devices Division stands proudly as a partner that customers can trust and meets their needs for optical device and microwave device products.

(2) Quality assurance strategy
To improve the quality of its semiconductor products and services, Compound Semiconductor Devices Division promotes overall optimization through the following activities:

<1> Assuring quality and reliability at design stage
In order to assure high quality and reliability at the design stage, Compound Semiconductor Devices Division adopts evaluation and analysis technologies supporting sophisticated designing environments and front-end technologies by thoroughly analyzing past problems.

<2> Assuring quality and reliability in production process
To prevent the creation and delivery of defective products and abnormal products, Compound Semiconductor Devices Division continuously improves its production processes and statistical management techniques, monitors the quality of its products, and takes thorough corrective actions if necessary, through original flow management.

<3> Improving customer satisfaction
In order to be recognized as a partner, Compound Semiconductor Devices Division actively seeks to satisfy its customers' various needs, over and beyond requirements for high-quality semiconductor products. Compound Semiconductor Devices Division also promotes the creation of mechanisms for conveying the voices of our customers smoothly to our manufacturing plants and keeping up with changing market demands.

(3) CS activities
Compound Semiconductor Devices Division performs various CS (Customer Satisfaction) activities every year to satisfy its customers. All Compound Semiconductor Devices Division's departments — marketing, sales, design, development, production, and staff — are involved in these activities in an attempt to supply optimum solutions to customers by accurately improving the elements of customer satisfaction, TQRDC (Technology, Quality, Responsiveness, Delivery, Cost).

Through these activities, Compound Semiconductor Devices Division translates the comments and opinions from its customers into improvements through feedback.
(4) Quality assurance organization

Figure 1-1 shows Compound Semiconductor Devices Division’s Quality Assurance Organization. As is conveyed by the expression “building in quality”, manufacturing divisions in various companies seek to continually improve their manufacturing parameters. Meanwhile, quality control divisions seek to carefully manage the quality of all product parts received at the factory, check the quality of manufacturing processes, maintain quality at the shipping stage, and provide services related to after-sales quality. To support these efforts, the factory superintendent (or General Manager) regularly holds quality conferences, quality checks are routinely carried out, and the quality and reliability of our products and services are thereby improved.

In order to execute focused management themes, achieve target values, and implement priority-based action plans based on our company’s quality policies and business policies, we carefully study factors such as field quality, production levels, and manufacturing process quality. In order to work collaboratively with our production companies and to further raise product quality, Compound Semiconductor Devices Division invites representatives of production companies and holds Quality Conferences hosted by our General Manager.

The following functions are performed by our Reliability and Quality Control Division, which is responsible for quality assurance company-wide.

(a) As the division that has overall control of production companies, this division helps introduce basic technologies, process development, and related technologies to production companies, and it also promotes lateral deployment of improvements and corrective actions in response to product quality-related issues.

(b) As the division responsible to customers for the quality of our semiconductor products, this division drafts plans concerning the quality and reliability of semiconductor products, performs quality and reliability testing and evaluation of products under development, maintains quality monitoring, and handles investigations and analyses of claims.

(c) As a business partner working to provide optimum solutions, this division plans, promotes, and implements activities to further raise company-wide CS (Customer Satisfaction) levels and to improve the overall quality of our business.
Figure 1-1. Overview of Quality Assurance Organization

General Manager

Sales Division

Product Development Division

Optical Semiconductor Devices

Compound Microwave Devices

Silicon Microwave Devices

Reliability and Quality Control Department

Domestic Manufacturing Companies
- NEC Kansai
- NEC Yamagata
- Kyushu Denshi Co., Ltd.
- Chuo Denshi Kogyo Co., Ltd.
- Naito Denssei Kogyo Co., Ltd.

Oversea Manufacturing Companies
- NEC Semiconductors (Malaysia)
- Microwave and Optical Semiconductors Tiwan Co., Ltd.

Quality Conference
Quality assurance system

In order to offer on a timely basis products that answer the needs of customers, Compound Semiconductor Devices Division has established and uses quality systems adapted to the demands of customers throughout the world that use international standards for quality assurance such as ISO9001 that cover the entire process from the product planning stage to development, design, trial production, evaluation, mass production, shipping and servicing. Figure 1-2 shows the quality assurance system.

First, in the planning stage, customer needs and wants are investigated in detail, and after the required product function outline has been established, concrete product development and design starts.

In the development and design stage, system design, circuit design, structural design, production method design, etc., are all conducted in parallel. Testing is particularly important in the design stage for complex and advanced IC design.

When the design stage is completed, a comprehensive design review (DR) is conducted by the Reliability and Quality Control Department and related departments.

At the end of product design, trial production begins. During the trial production stage, optimum manufacturing conditions are checked. After the attainment of the desired level has been confirmed through reliability evaluation tests and electrical quality testing, comprehensive evaluation is performed and then the process officially moves over to mass production.

In the mass-production stage, control using computers, and systems for quality information collection and feedback are being introduced and deployed in order to maintain uniform quality. Compound Semiconductor Devices Division also promotes TPM (Total Productive Maintenance) activities and SPC (Statistical Process Control) control as it is aware of the large influence these have on equipment reliability and product quality.

Compound Semiconductor Devices Division also performs parts and materials, production design, environment, instruments, and quality records control, quality-related education, training, and small-group activities for operators and engineers, as well as various activities based on ISO9001 quality systems such as for change and correction control.

Verification that there are no problems related to reliability in mass-produced products is done through long-term reliability testing using selected products, analysis of defects reported by customers and markets, and the findings are fed back to mass production or design.

These types of activities, in addition to being part of the organization of all areas involved in the quality assurance system as well as the individual level, also pass through the PDCA (Plan Do Check Action) cycle at various stages of the quality assurance process as part of promoting quality creation and maintenance improvement.

The basic purpose of the activities performed as part of this quality assurance system is to create a close partnership with the customer. Compound Semiconductor Devices Division attaches the utmost importance to such partnership with the customer.
Figure 1-2. Quality Assurance System

---|---|---|---|---|---
Market research | Engineering research | Product planning | New product development committee

Development

Design review

Trial production and evaluation

DS (Note) design review (design certification)

Trial production

Evaluation

Sample distribution

Reliability evaluation

New product sales committee

Trial production and evaluation

Mass-production trial and evaluation

Design review for mass-production

Evaluation

Sample distribution

Manufacturing

Order placement

Sales planning

Purchasing specifications

Production planning

Acceptance inspection

Manufacturing

Revision management

Shipments

Improvement measures

Product quality information

Warehousing

Final inspection

Market (in use)

Defects

Acceptance of complaints

Reception

Complaints investigations, analyses, and countermeasures

Response

Analysis reports

Note: DS stands for "Design Sample."
1.2 Quality Assurance in Product Development

1.2.1 General
Designing is an extremely important process for developing semiconductor device products that have functions, performance, quality, and reliability satisfying the needs of the customer. This section explains Compound Semiconductor Devices Division's product development, reliability designing, design review, and quality approval activities.

1.2.2 Product development
Compound Semiconductor Devices Division develops its products by using a quality assurance system that covers market research, understanding of the needs of the customer, assuring quality and reliability in each process of product design and development such as production, inspection, and testing, management of product delivery, and after-sales service.

Figure 1-2 illustrates Compound Semiconductor Devices Division's quality assurance system.

(1) Planning
Developing a new semiconductor device product begins with an understanding of the needs of the customer. These needs include the quality and reliability required by the customer, as well as the functions and performance required of the product. Based on an analysis of the technological trends in the market in question, competitiveness with the products of other makers, and business potential, a development plan is created and proposed. This development plan is created taking into consideration such factors as the development base technologies available inside and outside Compound Semiconductor Devices Division, new element technology development plan, and the quality and reliability technologies Compound Semiconductor Devices Division possesses, in an attempt to secure the targeted quality and reliability levels.

(2) Development design, evaluation of experimentally produced product, and mass production
Development of a semiconductor device product is designed prudently, based on the development plan created in the planning stage. The basic quality of the product is largely determined in the design stage. The design process of product development design are becoming increasingly complicated and diversified in recent years as finer semiconductor production processes are employed and the scale and density of the system to be integrated on the product are increasing. Against this background, the standardization of design tools, design techniques, and design libraries for accurately realizing the targeted product functions and performances and assure the intended reliability and quality is promoted, taking the capability of the production process into consideration, and such standardization applied to development design. To ensure and improve the designed quality itself, design review is carried out in the design process that is the core of development design. The points to be checked in that design process, such as observing the design rule, checking of the design and safety, and problems concerning reliability if any, are checked by highly qualified staff. After design review of the final process of development design, experimental production is started. During the experimental production, production variations are checked with respect to the production process capability, the characteristics of the experimentally produced product are thoroughly evaluated, and function evaluation and reliability test are conducted. If the experimental product satisfies the specified characteristics and functions, mass production evaluation is performed to check if the product can be mass-produced with stability, and reliability tests are conducted to check if the product satisfies specified quality grade. Production of the product is then approved. Mass production is started after these thorough and complicated processes.
1.2.3 Reliability design

(1) Basic reliability design concept

As semiconductor device products have increasing density and operation speed, production processes as fine as deep sub-micron are being increasingly employed to develop such products. As a result, the necessity of taking new factors, such as the stress factor of each element on the chip, into consideration has grown, and reliability design has become increasingly important to attain the quality and sophistication expected by the customer.

Compound Semiconductor Devices Division performs product development by incorporating reliability design in the product development flow.

Basically, the reliability of a semiconductor device product is backed up by each part (such as element on chip, chip itself, and package) constituting the product. To secure and improve the reliability of the product, therefore, the reliability of the constituent elements must be harmonized.

Generally, reliability is divided into three stages, the early failure stage, the random failure stage, and the wear-out failure stage, as expressed by the bathtub curve. At Compound Semiconductor Devices Division, early failures are eliminated through proper screening, while random failures are eliminated through production process control. To eliminate wear-out failures, Compound Semiconductor Devices Division implements reliability design in the diffusion process, package development stage, and circuit layout designing, and ensures product life (time until wear-out failure) so that products being used in the market do not reach wear-out failure.

We work to maintain quality and reliability through activities such as process monitoring during the product development process to ensure reliability by controlling variations among manufacturing processes.

The reliability design described above consists of activities built in the product development process to ensure reliability enabling customers to use with peace of mind products that are designed with wear resistance for the failure modes indicated in Chapter 3, while maintaining main electrical performance. If the customer requests a special quality level, an original product development program that meets the required quality level is prepared and development and production in all processes from the product development stage to mass production are managed based on this program. ISO/TS16949: 2002 is an example of such a program for automotive products. In product development in response to such a request from the customer, management is performed in each development process, including product planning, system design, circuit design, trial production, evaluation, and mass production, so as to meet the request, and development is performed in close communication with the customer.
(2) Reliability designing related to basic elements of product such as production process and package

Basically Compound Semiconductor Devices Division’s reliability design consists of the concept of preparing a “design standard” based on reliability simulation, test data, evaluation results, and quality monitor data and implementing product design based on the above to secure reliability for each product. “Design standards” are prepared using the following procedure for the diffusion process/packaging (assembly) according to the production process.

(a) Production process reliability design

<1> The customer’s requests (including reliability and quality) are clarified before the quality and functions are developed, taking into consideration technological trends in the target market for which the product is intended, superiority over competitors’ products, and business potential. This clarifies the level of the constituent element to be realized in the process, and each target characteristics, performance, and reliability of the chip. Afterward, development is performed using the following procedure.

<2> If a new diffusion process is developed, an evaluation TEG (Test Element Group) chip is developed that enables observation of deterioration in the failure modes described in Chapter 3 using accelerated tests. The failure mode is selected each time depending on the characteristics and performance of the diffusion process. In doing so, the major parameters such as electronic migration of the aluminum wiring, TDDB of the oxide film, hot carrier of transistors, leakage current, aluminum slide, retention characteristics of the memory elements, and ESD/latchup are evaluated. At this time, evaluation grade that takes variations of production process during mass production is taken into account in selecting the TEG chip, and the product is experimentally produced and evaluated.

<3> The accelerated tests using the TEG chip described above are performed, and the converted life under real use conditions is checked.

<4> If the calculated service life is acceptable, a “design standard” is created from the evaluation grade. The “design standard” prepared here defines the basic characteristics, wiring capacitance, element layout dimensions, etc., and the points to be observed while layout design of the chip is performed. At this time, the specification conditions of the production process are also determined so that the characteristics of the elements defined by the design standard are correctly and accurately secured and controlled. If the target characteristics of the service life have not been attained, the specifications are reviewed (feedback regarding problems) from the viewpoints of production process flow and production conditions, and evaluation and improvement are made until the desired characteristics are obtained.

(b) Package reliability design

If a new semiconductor IC package is developed, the TEG is created by incorporating a chip having the basic electrical characteristics in that package, and accelerated environmental testing is conducted to check board assembly heat resistance (thermal stress during mounting) and environmental durability (thermal stress and mechanical stress) to confirm that the package will be free of problems even when it is put into practical use. A design standard to design the actual product is then prepared. (Accelerated environment testing is performed based on worldwide standards such as MIL-STD-883.) The term “design standard” prepared here applies to the package materials, the rule employed for wire bonding or chip mounting, the thermal resistance calculation rules, etc., and describes items that must be observed during design of the package of the chip.
1.2.4 Design review

Design review in development and designing semiconductor device products of Compound Semiconductor Devices Division is done to check if the designed product complies with the “design standard” when the design process, which is the core of development and designing, is completed, if the related design rules are observed, if the design specifications, which are the input for the design, are correctly met, and if the lessons learned from the defects that occurred in the past are correctly reflected, so that the next design process can be started.

Design review of development and design is executed at various examination meetings, depending on the design schedule. In this series of design review actions, the largest milestone is “design review for starting experimental production of a new product”, which is explained below.

In accordance with the new product development system illustrated in the quality assurance system diagram in Figure 1-2, a newly design product that has gone through each layer of design, such as system design, circuit design, and layout design, is thoroughly examined by this design review. By using the designed product that has passed this examination (i.e., mask pattern data), experimental production for checking the characteristics and functions of the new product is started. Since trial production of a new product requires processes such as the manufacturing of masks for trial production, trial diffusion, and trial package assembly, any failure of the trial product needs to thoroughly be eliminated through feedback (additional round of trial production). In this design review, therefore, personnel from the department in charge of development and the department of each specialty (such as process, assembly, and production) participates to check if the design standards and rules for securing the specified reliability and quality, and for product safety and applied diffusion process are met, if the applied package assembly standard is observed, and if the intended functions and performances are secured.

1.2.5 Product qualification

Quality approval for the semiconductor device products of Compound Semiconductor Devices Division is to check if the functions, performance, electrical characteristics, reliability, and quality of the experimentally produced product are at the level intended at the product planning stage, if the product quality level is sufficient to satisfy the customer, and if it is all right to start the mass production of the product. Basically, the mass production stage cannot be started unless quality approval is completed. Quality certification is conducted both in-house by Compound Semiconductor Devices Division and by the customer. Compound Semiconductor Devices Division’s in-house quality certification is described below.

Outline of procedure for approving quality

Quality approval conditions differ depending on the newness of each part (such as element on chip, chip, and package) that constitutes the product under development. For example, if elements such as the production process, production line, and package are completely new, and these new elements are applied for the first time to the product under development, the most stringent reliability and quality evaluation is included in the approval condition. On the other hand, if the reliability and quality of the process and package have been already tested and proved during development of products already released, the approval condition to be applied is not as stringent as above. This is because the reliability of a product is basically backed up by the production process and package, and if these can be checked at each production line, the quality of the successor products is approved by evaluating the reliability and quality of the products, placing emphasis on the circuit configuration and layout, which differ from one product to another.

The system to approve new products is explained next.
(1) Certification of new products

The process from quality certification to mass production is implemented using the following procedure. See Figure 1-3 for a schematic diagram.

**Figure 1-3. Outline of New Product Qualification**

- Trial production of new product
- Function and performance evaluation
- Mass productivity evaluation
- Reliability evaluation based on reliability and quality standard
- Quality certification
- New product sales committee
- Mass production

(a) Evaluation based on reliability quality standard

Reliability evaluation based on the reliability quality standard defined in advance is performed by using an experimentally produced product. The reliability quality standard is defined to fully satisfy the customer’s requirements under the actual operating conditions, and is determined based on comprehensive evaluation of the quality and reliability levels requested by the customer, the results of surveys on similar products available on the market, and the current technological standard, and consists of the following major elements.

- Initial-phase defect rate
- Market defect rate
- Reliability evaluation items and conditions
- ESD/latchup/noise resistance/SER
- Test coverage
- Others

A quality assurance program is created by preparing three major standards, “Standard”, “Special” and “Specific”, in advance, from which the customer can choose depending on his/her requirements.
(b) Evaluation of trial production products (function and performance evaluation, mass-production productivity evaluation)

Various characteristic evaluation tests are conducted by using the trial production product, taking into consideration whether the product satisfies the intended specifications, such as functions and performances, and production margin during mass production. If any problem concerning mass production is found as the result of producing the experimental product, specific actions such as feedback to the product design department or production process are taken, improvements are made, and whether the problem has been correctly solved is checked by re-evaluating the product on which improvements have been made.

(c) New product sales committee

This committee examines the result of evaluating the experimentally produced product, testability such as the test program to be applied to product inspection during mass production, the result of evaluating the production cost model, and other parameters necessary for starting mass production. The participants in this meeting include members from the related departments such as marketing, applied technology, product designing, production, and reliability. They confirm that the needs and requests of the customer are satisfied, and conduct a thorough study so that mass production can be smoothly started. Basically, only products that have passed the review go to the next stage of mass production.
1.3 Change Management

(1) Process change management

The design and process of a semiconductor device are constantly changed to improve functions, quality, reliability, and productivity. When these changes are made, thorough evaluation and initial-phase drift control are conducted, and efforts are made to prevent occurrence of quality-related problems as a result of changes. Figure 1-4 shows the change management flow. If a change is planned by the engineering department, a change plan is created and examined and evaluated by the related departments. Then a change petition is prepared and reviewed, the change is performed, and the result of initial-phase drift control is checked.

Figure 1-4. Change Management Flow

Change plan and review of a change petition are designed to prevent quality accidents, taking the following into consideration.
• Change contents (merits and demerits)
• Influence on product quality
• Evaluation of contents
• Items (characteristics, reliability)
• Product identification
• Study of side effects
• Change schedule
• Customer notification

As technological evaluation, reliability evaluation using the TEG or product evaluation is performed. The change petition is reviewed by the related departments, and whether mass production can be started or not is determined from the result of technological evaluation.
Depending on these results, the change petition is prepared and reviewed, and the change is implemented. After the change, initial-phase drift control is performed, and the effect of the change is checked.

(2) Notification of changes to customers (PCN: Product Change Notice)
(a) Products manufactured under the new process flow are shipped to customers only after they have acknowledged receipt of the P.C.N.

(b) P.C.N provides to customer detailed information and instruction on the following topics.
   - Product name
   - Change contents
   - Reasons for change
   - Influence on quality and evaluation result
   - Change period
   - Identification

Note  Non major or critical change does not provide P.C.N. to customers.
1.4 Standards System and Control

It is extremely important to standardize and observe the rules, criteria, and methods to be shared by all relevant divisions to (1) systematically plan, design, produce, and sell semiconductor products, (2) respond to customer needs, and (3) ensure product quality.

Compound Semiconductor Devices Division uses information on customer needs and the results of market surveys as well as engineering developments as a basis for providing customers with products that satisfy in terms of high quality, adequate cost, and prompt delivery. These practices have been standardized and promoted as a unified system of rules shared by all relevant divisions.

For the establishment of standards, not only customer requirements but also international standards, methods and requirements are taken into consideration whenever possible to ensure satisfaction among customers worldwide. Figure 1-5 outlines the standards system in Compound Semiconductor Devices Division. These standards are mainly control standards, product design standards, and manufacturing standards.

![Figure 1-5. Standards System](image_url)
Compound Semiconductor Devices Division has many semiconductor manufacturing companies in Japan and overseas. Each of these companies creates and issues its original standard system.

However, adequate consideration is given in creating and observing standards so that the same product has uniform quality regardless of the production companies that produced it.

Compound Semiconductor Devices Division defines the basic items and product specifications that affect the quality of products, and each manufacturing company defines the implementation specifications.

Figure 1-6 shows the relationships among the standards of Compound Semiconductor Devices Division and its manufacturing companies.

The standard systems and standards need flexibility to adapt to technological innovation and rational management technology.

These standard systems and standards are actively enacted and revised in order to include corrective measures and preventive actions, rationalization, and optimization that are considered necessary for coping with accidents and improvement activities, so as to satisfy time requirements.

In recent years, the standards that were available as paper documents have been increasingly replaced by electronic documents, so that they can be distributed more quickly and accurately, and use of electronic systems has been promoted in an attempt to completely eliminate paper documents.

Numbering, issuing, and transfer management of standards, and disposal of the standards that have become obsolete are carried out by a management department. This department organizes electronic specification management systems, and performs management and distribution of new editions and collection and disposal of old editions.

Therefore, products and specifications always match and are traceable.

Standards are considered as product safety (PS) documents and stored by the management department.
1.5 Purchased Parts and Materials and Control of Purchased Products

Continuing stable production while maintaining quality and reliability requires securing necessary high-quality parts and materials and purchased products. For strict selection of suppliers, parts, materials, and purchased products, Compound Semiconductor Devices Division employs a vendor approval system.

To select vendors and parts and materials, sample creation evaluation, quality verification test, and audit of quality assurance system and production process control condition are performed.

The quality of the purchased parts and materials and purchased products is assured by conducting an acceptance inspection. In addition, periodic check of the vendor’s quality is conducted to maintain and improve the quality.

Quality assurance of purchased products also includes incoming inspections and periodic quality audits for manufacturing company, through which quality is confirmed and guidance is provided to the vendors.

Parts, materials and products are stored under the appropriate environment in accordance with Compound Semiconductor Devices Division's regulations, so that aging does not occur during storage and the quality of the stored parts, materials, and products is assured.

1.6 Quality Assurance System with Manufacturing Company (Affiliates and Cooperative Companies) and Subcontractor Management

As part of its quality assurance system, Compound Semiconductor Devices Division concludes quality assurance contracts with production companies (affiliates). These contracts clearly specify the distribution of roles and responsibilities among the companies. The quality control division in each production company performs its own process control. In the future, Compound Semiconductor Devices Division plans to introduce a management system that includes a network for sharing this process control information as on-line data. Figure 1-2 illustrates the quality assurance system applicable to our quality assurance division and production companies.

This system, which is compatible with “pull production” systems, implements preventive and corrective measures through close cooperation among our companies, resulting in solid quality assurance.
1.7 Product Identification and Traceability

Product identification is controlled by making production lot code markings to products and their manufacturing history can be traced. Compound Semiconductor Devices Division standard marking is shown below. Part of the standard markings in cases omitted due to package size, etc., there are some cases where the markings are expressed by color codes and not by alphanumeric characters.

- **Example of Product with Manufacturing Week Code Marked**

```
02 010 *****
```

- **Example of Product with Manufacturing Month Code Marked**

```
2 9 *****
```

Based on the international standard ISO-8601, the first week of the year is one that includes the first Thursday of that year.
1.8 Manufacturing Quality Assurance System

1.8.1 Outline

(1) Quality assurance in manufacturing processes
Semiconductor device manufacturing processes include wafer processes in which basic elements and circuit patterns are configured on wafers, and assembly processes in which the semiconductor devices are finished. To verify quality after manufacturing, electrical characteristics tests are performed after wafer processes and assembly processes.
In order to build in quality in the manufacturing processes, a results check of products at each stage in the manufacturing process is performed. Daily inspections and periodic maintenance of manufacturing equipment are performed. Statistical process control (SPC) through control charts is also implemented for important parameters and improvement activities are conducted to maintain variation-free production at all times.
Items which influence quality in the manufacturing process include, in addition to process variations, defects from dust particles and destruction of the insulation layer by static electricity, and improvements in these areas are being made continuously. In the wafer processes in particular, efforts are promoted to reduce the generation of dust by equipment in order to maintain a high level of cleanliness and work is performed in clean rooms with dust-proof clothing to further enhance dust-free working conditions.
Equipment is grounded, and conductive floors and shoes are provided in addition to prevent workers from static charge as countermeasures for static electricity.

(2) Line certification
When a new semiconductor device manufacturing line is inaugurated and begins production, a line audit is conducted and standards, work, maintenance, environment, and layout conditions are confirmed together with reliability evaluation results from prototype products, and the line is certified. If there are problems, countermeasures are implemented to make the necessary improvements.

(3) Line assurance
Together with periodic checks of the equipment and operations in each individual process, it is possible to reduce fluctuating factors and improve process capacities to create conditions where only good products will be produced. If this is done, checks need not be conducted for each lot, and it becomes possible to assure the quality of products produced by the line as a whole. This condition is called line assurance, and this is already being implemented on some lines.

1.8.2 Wafer processes
An outline of wafer manufacturing processes and an example of a quality control flow chart are shown in Figure 1-7.
Figure 1-7. Outline of Wafer Manufacturing Process and Quality Control (with silicon IC as an Example)

<table>
<thead>
<tr>
<th>Process</th>
<th>Control Item</th>
<th>Control Objective</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Wafer</td>
<td>Resistivity</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td></td>
<td>Thickness</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Warp</td>
<td></td>
</tr>
<tr>
<td>Well Formation</td>
<td>Appearance</td>
<td>Monitoring of film thickness</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td>Layer resistance</td>
<td>Confirmation of ion implantation volume</td>
</tr>
<tr>
<td>• Ion implantation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Diffusion</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Element Separation</td>
<td>Film thickness</td>
<td>Monitoring of film thickness</td>
</tr>
<tr>
<td>• Film deposition</td>
<td>Appearance</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td>Dimensions</td>
<td>Monitoring of pattern dimensions</td>
</tr>
<tr>
<td>• Etching</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Oxidation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Oxidation</td>
<td>Film thickness</td>
<td>Monitoring of oxidation film thickness</td>
</tr>
<tr>
<td>Gate Electrode Formation</td>
<td>Film thickness</td>
<td>Monitoring of film thickness</td>
</tr>
<tr>
<td>• Film deposition</td>
<td>Appearance</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td>Dimensions</td>
<td>Monitoring of pattern dimensions</td>
</tr>
<tr>
<td>• Etching</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD Area Formation</td>
<td>Appearance</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td>Layer resistance</td>
<td>Confirmation of ion implantation volume</td>
</tr>
<tr>
<td>• Ion implantation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Hole Formation</td>
<td>Film thickness</td>
<td>Monitoring of film thickness</td>
</tr>
<tr>
<td>• Film deposition</td>
<td>Appearance</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Etching</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal Formation</td>
<td>Film thickness</td>
<td>Monitoring of film thickness</td>
</tr>
<tr>
<td>• Aluminum spatter</td>
<td>Appearance</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td>Dimensions</td>
<td>Monitoring of pattern dimensions</td>
</tr>
<tr>
<td>• Etching</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Passivation Formation</td>
<td>Film thickness</td>
<td>Monitoring of film thickness</td>
</tr>
<tr>
<td>• Film deposition</td>
<td>Appearance</td>
<td>Confirmation of shape</td>
</tr>
<tr>
<td>• Photo lithography</td>
<td>Film quality</td>
<td>Control of film quality</td>
</tr>
<tr>
<td>• Etching</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Element Characteristics</td>
<td>Electrical characteristics</td>
<td>Pass/fail judgment of electrical element characteristics</td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wafer Inspection</td>
<td>Electrical characteristics</td>
<td>Pass/fail judgment of electrical operation, performance</td>
</tr>
<tr>
<td>Wafer Warehousing</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The completion of IC chips on wafers begins when silicon wafers, compound semiconductor wafers and other parts and materials are received. They pass through several hundred processes, such as film deposition, pattern formation, and ion implantation, heat treatment and other processes repeatedly. In all of these processes, process checks are conducted, with the equipment condition and product results being confirmed, and in each process, the incorporation of quality is assured.

(1) Film deposition process
The film deposition process consists of the oxidation, chemical vapor deposition (CVD), spatter and other processes.
In the oxidation process, since the heat processing temperature is an important parameter, thermocouple control for controlling the equipment is strictly carried out and the treatment temperature and oxidation film thickness are controlled.
In the CVD process, together with control of the film deposition temperature and gas flow volume, the film thickness, refraction rate and etching rate, etc. are used to control the film quality.
The spatter process is a process where a metal film such as aluminum is formed. In order to maintain the reliability of the aluminum metal, the equipment's vacuum, temperature, etc. are controlled. The results are monitored by measuring the film thickness and checking the film quality.

(2) Photo lithography process
Processing of the film created in the film deposition process is accomplished in the photo lithography process. Ordinarily, the photo resist process and etching process are included, but here, the photo resist process will be explained. The photo resist process consists of the photo resist coating process, the mask pattern exposure process and the development process, and this forms the photo resist pattern on the film which has been formed. In order to preserve the pattern dimensions and formation in the correct condition, the photo resist film thickness in the coating process and the exposure intensity and lens focusing position, etc. in the exposure process are carefully controlled.

(3) Etching
The process whereby the film formed on the wafer with photo resist pattern as a mask is processed and removed is called etching. The speed of etching is controlled so that not too much film or not too little film is removed.

(4) Ion implantation
The ion implantation process is a process whereby the wafer surface is bombarded with impurities such as phosphorous or boron to control the Vt voltage which is the main characteristic of diffusion layer formation and MOS transistors. In order to control the implantation volume, the layer resistance, etc. of the diffusion layer is monitored.

(5) Diffusion process
The process whereby the impurities implanted in the film and in the silicon substrate are activated and their range broadened is called the diffusion process. The temperature and time are controlled and the layer resistance, etc. is monitored.

(6) Wafer inspection
When the wafer manufacturing process is completed, first, in the element characteristics inspection, the basic characteristics of the transistors is checked, then the wafer inspection is conducted and a pass/fail judgment is rendered on whether each of the chips on the wafer operates normally electrically speaking. After identifying defective chips, they are removed in later processes. Chips which have been found to be highly reliable in the wafer inspection in addition to successful formation in the process are placed in storage as semi-finished products.
1.8.3 Clean activities in the manufacturing process

Activities to clean the manufacturing process have a favorable influence on the quality and reliability of semiconductor products and are directly related to the number of chips obtained from a wafer, i.e. the yield. This influences Compound Semiconductor Devices Division's cost as well as the purchasing price for the customer. Therefore at Compound Semiconductor Devices Division, we are making every effort to incorporate clean activities in important technological activities.

(1) Level of cleanliness

There are cleaning standards of the International Organization for Standardization (ISO14644) and Federal Specifications and Standards (U.S.) (FED-STD-209D). The latter are generally used in Japan. Table 1-1 shows the Federal Specifications and Standards.

Table 1-1. Level of Cleanliness

<table>
<thead>
<tr>
<th>Cleanliness Class</th>
<th>Number of Particles of Dust (0.5 μm or Larger)</th>
<th>Example of Applicable Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 1</td>
<td>1/Cubic Foot</td>
<td>Lithography, diffusion, metallize, etc.</td>
</tr>
<tr>
<td>Class 10</td>
<td>10/Cubic Foot</td>
<td>Diffusion, metallize, etc.</td>
</tr>
<tr>
<td>Class 100</td>
<td>100/Cubic Foot</td>
<td>Diffusion, metallize, etc.</td>
</tr>
<tr>
<td>Class 1000</td>
<td>1000/Cubic Foot</td>
<td>Power room, holding room, changing room, etc.</td>
</tr>
<tr>
<td>Class 10000</td>
<td>10000/Cubic Foot</td>
<td>Power room, holding room, changing room, etc.</td>
</tr>
</tbody>
</table>

(2) How to achieve sufficient cleanliness

(a) Guaranteeing cleanliness

<1> Plant design

Clean air can be assured for the work shop by drawing air in from outside the plant, filtering it and delivering it to the work rooms, in addition to making the work shop positively charged and preventing dust from entering in through the cracks in walls and doors. To achieve Class 1 to 10 cleanliness, an all down flow system, in which the entire ceiling is fitted with filters and air is exhausted through the floor, is utilized.

<2> Reduction of dust generated by humans

Human dust is generated in large quantities from human workers and countermeasures against such dust must be taken. The main sources of human dust are fibers from the clothes workers wear, and shed dead shin, hair, and makeup. To reduce such human dust, workers at Compound Semiconductor Devices Division wear protective clothes.

<3> Line automation

To prevent human dust from affecting the quality of products, Compound Semiconductor Devices Division promotes automation for the transportation of products and processing lines in order to maintain a high level of cleanliness. Also, by completely separating the area where people work from the area where products are conveyed and processed, even greater levels of cleanliness are being achieved.

<4> Response to contamination of the atmosphere in the clean room

With improvements in large scale integration and the development of ultra-miniaturization, efforts are being made to upgrade cleanliness to the level of molecules and atoms that pass through the filter, and with the idea of distinguishing these from particles of dust, to make improvements in “Clean Room Atmospheric Contamination.”
(b) Reducing equipment dust generation

Since the foreign particles generated by manufacturing equipment during product processing have a great influence on product yield and quality, at Compound Semiconductor Devices Division, we are putting our energies into reducing the dust generated by equipment. The results of these improvements are always being developed at other manufacturing companies as well.

1.8.4 Assembly processes

Figure 1-8 shows an outline of the semiconductor device manufacturing (assembly) process and an example of a quality control flow chart.

Beginning from the wafer and assembly materials receiving inspection, and extending to the final product inspection, important control points in the manufacturing process are decided on. These points are monitored continuously and through the methods of taking countermeasures for abnormalities, quality assurance activities are implemented.

On each manufacturing line, the following type of process check specifications, with detailed control items decided for each process, are prepared and put into effect.

Process check items can be roughly divided into those related to setting of working conditions and items related to product results, and check methods for each respective control item, check frequencies, recording methods, etc. are stipulated and detailed control is enforced. Also, the working environment in the manufacturing process, which exerts such a great influence on reliability and quality, particularly temperature, humidity, dust, and DI water, are important control items, and check methods, frequencies and recording methods, etc. are clearly specified.
### Figure 1-8. Outline of Assembly Process and Quality Control (with Plastic PKG as an Example)

<table>
<thead>
<tr>
<th>Process</th>
<th>Control Item</th>
<th>Control Objective</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer</td>
<td>Appearance</td>
<td>Removal of wafer breakage, chipping</td>
</tr>
<tr>
<td>Dicing</td>
<td>Appearance, Pure water resistivity</td>
<td></td>
</tr>
<tr>
<td>Chip appearance</td>
<td>Appearance</td>
<td>Chip appearance pass/fail judgment</td>
</tr>
<tr>
<td>(Breakage, nicks)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mount</td>
<td>Wettability</td>
<td>Mounting stability</td>
</tr>
<tr>
<td>Mount appearance inspection</td>
<td>Appearance, Bonding strength</td>
<td>Mount pass/fail judgment</td>
</tr>
<tr>
<td>Wire</td>
<td>Temperature</td>
<td></td>
</tr>
<tr>
<td>Bonding</td>
<td>Appearance, Tensile strength, Shear strength</td>
<td>Bonding pass/fail judgment</td>
</tr>
<tr>
<td>Bonding appearance inspection</td>
<td>Temperature, Time, Wire flow</td>
<td>Mold sealing pass/fail judgment</td>
</tr>
<tr>
<td>Mold sealing</td>
<td>Ingredients, Temperature, Plating thickness</td>
<td>Assuring finish quality</td>
</tr>
<tr>
<td>Lead surface finishing</td>
<td>Appearance</td>
<td>Marking pass/fail judgment (Marking position, Legibility)</td>
</tr>
<tr>
<td>Marking</td>
<td>Appearance inspection</td>
<td>Removal of lead formation defects</td>
</tr>
<tr>
<td>Sorting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead forming</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Final inspection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Warehousing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shipping</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Technical Note PQ10478EJ02V0TN
(1) Dicing
In the dicing process, not only are the chips checked in the appearance inspection for chip surface flaws and contamination, but quality control is implemented through confirmation of the cutting width and cutting conditions after dicing. The major control items in working conditions that are confirmed periodically are the flow volume of cutting and cleaning water, the cutting speed and cutting blade replacement frequency. The resistivity and water pressure of DI water, which have a great influence on reliability, are also controlled at a constant level.

When a scribing method is used for chip dicing, quality control is performed by checking the post-scribing quality of grooves on wafers, chip cleavage after breaking, and damage from pressure on chip surfaces.

(2) Mounting
In the mounting (die bonding) and mount baking processes, control of the chip mounting temperature, compression load, inert gas flow volume, baking temperature, and timing, etc. are controlled. Not only are the standards for amount of adhesive and wettability monitored when checking product reliability, but periodically, bonding strength tests are performed, with mounting conditions being controlled based on the results.

(3) Bonding
A large number of parameters is controlled in the working conditions in the bonding process. In particular, the bonding load, temperature, and ultrasonic wave level are set minutely for each product.

In bonding appearance, abnormalities, poor adhesion, shorting or curling of wires, or other defects are monitored for the ball shape in particular. In addition, on the point of product reliability, wire tensile strength and ball shear strength are measured periodically and controlled based on the results.

(4) Molding, curing
In the molding process, temperature is an extremely important parameter, and even with the modern auto molding equipment, which makes it possible to control conditions so the temperature will not deviate from the set temperature, measurements are taken periodically and the temperature at each point is maintained within a fixed range at all times.

In the area of product reliability, first of all, through control of the characteristics of the resin raw material, the attempt is made to stabilize product quality. Also, following mold sealing, the inside of the package is checked periodically by X-ray photography, and voids, burrs, and chipping in the mold surface and flaws in the lead frame, etc. are checked for in the appearance inspection. Also, through mold curing at controlled temperatures and timings so as to prevent there being any resins which haven’t reacted, efforts are made to improve reliability.

(5) Lead surface finishing
Pre-processing conditions and cleaning requirements are specified in detail for controlling plating conditions to ensure the quality of finished leads. Particularly, current values, plating time, solution temperature and composition are monitored continually so that they are performed under constant conditions.

From the point of product control, confirmation of plating thickness, composition, appearance, solderability, plating hardness, and plating adhesion are performed periodically.

(6) Markings
Markings on products include the product name, manufacturing plant, date of manufacture and other inherent information. The most commonly used marking method is laser marking, which has the advantage of being stronger than ink. The depth of markings made by laser is controlled by the laser power and depths are set which present no problem to the reliability of the product. In-process control includes not only checking for the
presence of markings, position and orientation through automatic recognition by machine, but also checks for
imperfections, nicks or blurring, etc. in the marking in the visual appearance inspection.

(7) Lead forming
This is a process which has a great influence on the mountability of a product on a circuit board in its molded
condition, and since it is the final assembly process, the major dimensions are checked. Leads in particular
are monitored in the appearance inspection or using automatic visual inspection equipment. Control items are
bending of leads and lead flatness, etc. Also, in order to prevent lead forming defects from resin or solder
residues, the metal dies are cleaned periodically and quality control is performed.

1.8.5 Static electricity countermeasures
At Compound Semiconductor Devices Division, various types of countermeasures are taken to prevent degradation
or destruction caused by static electricity in the manufacturing process. Some examples of the countermeasures
taken are shown below.

(1) Examples of countermeasures in the working environment

<table>
<thead>
<tr>
<th>Item</th>
<th>Example of Countermeasure</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Relative humidity control</td>
<td>Controlled at a minimum of 40%.</td>
</tr>
<tr>
<td>• Grounding of floors and work benches</td>
<td>Conductive floors, implementation of conductive sheets, ground connecting lines, etc.</td>
</tr>
<tr>
<td>• Removal of insulators and dielectrics</td>
<td>Countermeasures are taken to eliminate plastic and other work materials that</td>
</tr>
<tr>
<td></td>
<td>anti-static treatment, and anti-static coating are applied, etc.</td>
</tr>
</tbody>
</table>

(2) Examples of countermeasures for equipment, jigs and tools

<table>
<thead>
<tr>
<th>Item</th>
<th>Example of Countermeasure</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Equipment grounding</td>
<td>Ground connecting lines.</td>
</tr>
<tr>
<td>• Storage shelves, carts, etc.</td>
<td>Implementation of conductive sheets, earth chains, etc.</td>
</tr>
<tr>
<td>• Use of anti-static containers, etc.</td>
<td>Anti-static containers are used for storage of semiconductor devices.</td>
</tr>
</tbody>
</table>

(3) Examples of countermeasures for workers

<table>
<thead>
<tr>
<th>Item</th>
<th>Example of Countermeasure</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Human body (worker) grounding</td>
<td>Wrist straps, conductive shoes, finger sacks, aprons and anti-static work clothing, etc. are used.</td>
</tr>
</tbody>
</table>

On the other hand, static electricity has the characteristic of attracting dust, etc., and at Compound
Semiconductor Devices Division, checks are performed periodically in an attempt to maintain the effects of
countermeasures.
1.9 Sorting and Inspection Quality Assurance System

Here, we explain concerning the final process, which is the sorting and inspection quality assurance system.

(1) **Electrical sorting**
All products with latent defects, and products which have been found to be defective in the diffusion and assembly processes, are checked electrically and removed, so initial quality is assured.
This electrical sorting is ordinarily performed at room temperature.

(2) **Screening test**
In cases where customers determine that products with higher quality would be desirable, burn-in tests are performed, and products that exhibit faulty operation after high-temperature bias tests are eliminated.

(3) **MRT**
Samples are taken from product groups and are subjected to reliability tests.
In this way, quality is assured and if defects occur, they are analyzed and the defect information is fed back so that improvements can be incorporated in the manufacturing process.

(4) **Final inspection**
The final inspection process is conducted to determine whether the sorting process carried out above was done correctly or not.
A predetermined number of samples is taken from a lot which was manufactured under the same conditions, and judgment is made as to whether that lot is good or defective. At Compound Semiconductor Devices Division, the LTPD sampling method is used.
1.10 Control of Equipment and Measuring Instruments

(1) Equipment control
Semiconductor manufacturing equipment is required to be highly accurate and highly reliable, so investigations are conducted beginning at the design stage when new equipment is to be introduced. The equipment is then completed with the specified characteristics built in.
Also, for mass production equipment, before beginning their use, startup checks, daily checks and periodic checks, etc. are decided, and checks are conducted based on these check lists.

(2) Measuring instrument control
Calibration of measuring instruments and meters is entrusted to a specialized department or company. Measuring instruments used in calibration are linked with national standards.
Also, the calibration frequency is decided for each piece of equipment and consideration is also given to the repeatability accuracy.
A label specifying the period of validity is affixed to each instrument after it has been calibrated.
In addition, core equipment is controlled separately one unit at a time by the equipment control department, which keeps it calibrated until the period of validity expires.
Links with national standards are shown in Figure 1-9.
Figure 1-9. Traceability of Measuring Instrument and Meters

[Measuring instruments]

International Committee of Weights and Measures

Agency of Industrial Science and Technology, Electrotechnical Laboratory

Communication Research Laboratory

Japan Quality Assurance Organization

Japan Electric Meters Inspection Corporation

High frequency standard instruments

DC and low frequency standard instruments

Frequency and time standard instruments

Measuring instruments at each factory

[Meters]

International Committee of Weights and Measures

Agency of Industrial Science and Technology, National Research Laboratory of Metrology

Japan Society for the Promotion of Machine Industry

Nippon Kaiji Kyokai (Japan Marine Society)

Japan Quality Assurance Organization

Standard instruments for microscopes, length, weight, pressure, etc.

Meters at each factory
1.11 Control of Defective Products

In the case that defective products which deviate from control standards occur in the manufacturing process, the following measures are taken.

- Good products and defective products are separated.
- They are disposed of in accordance with predetermined rules.
- They are kept together with quality records and utilized as examples in improvement activities.

The flow of treatment of faulty products at Compound Semiconductor Devices Division is shown in Figure 1-10.

Figure 1-10. Flow of Abnormal Processing
1.12 Preventive Activities, Corrective Measures

(1) Preventive activities
In the design process, examples from the past are analyzed and the results are fed back into design standards, guidelines, etc. so that the same mistake will not be made again.
For details, please refer to Quality Assurance in Product Development (see 1.2).
In order to prevent abnormalities in the manufacturing process before they happen, a new product introduction investigation and equipment design investigation are conducted before new products and new equipment are introduced on a line, and their specifications are confirmed for appropriateness to volume production.
For important processes, prototype production and TEG are conducted and conditions are optimized so that the optimum conditions are delivered on the line.
Side effects are also carefully predicted and confirmed, so that trouble is prevented before it takes place.
In order to prevent trouble from occurring due to deterioration or changes in equipment, daily equipment inspections and periodic maintenance inspections are carried out.
Improvement activities are also promoted through TPM activities, etc. to prevent equipment trouble organizationally before it can occur.

(2) Early discovery
Important parameters for early discovery of troubles with equipment or products are controlled through control charts so that tendencies toward abnormality can be discovered early. Also, through improvements in the accuracy of measuring equipment, review of process check methods and improvements in in-process monitoring, etc., improvement activities are positively promoted relating to detection of abnormalities so as to respond to minute developments and greater sophistication of manufacturing processes.
Preventive activities are performed through feedback not only to manufacturing but also to design and production engineering.

(3) Treatment of abnormalities
If an abnormality is discovered in the control items of any process among the manufacturing processes, the scope of the countermeasures for the abnormality are investigated, quality checks of the affected lot are performed according to predetermined treatment procedures and flow of the faulty products is prevented. At the same time, the cause of the trouble is investigated and countermeasures, together with recurrence prevention activities are implemented.

(4) Horizontal development
Concerning serious process abnormalities, the related departments conduct a case analysis, to dig in to determine the cause of the trouble, then institute countermeasures to prevent recurrence and carry out horizontal development on other related lines, thus preventing the same kind of trouble occurring on other lines before it can occur.

The above activities are all recorded as quality records.
The flow of horizontal development procedures is shown in Figure 1-11.
Figure 1-11. Flow of Horizontal Development

- Quality problem
  - Claim
  - Result of improvement
- Accident prevention measures
- Request from customer

Horizontal development registration

Development unnecessary

Answer to request issuer

Judgment on handling of horizontal development/information development

Horizontal development

Information development notice

Status check, evaluation and implementation of countermeasures

Evaluation and implementation results feedback

Trace result report

Completion
1.13 Logistics Quality Assurance System

In order to deliver products with the required quality in response to customer orders, quality assurance at the distribution stage is indispensable. A representative example of the logistics flow of semiconductor devices is shown in Figure 1-12. Quality assurance activities in distribution include packaging design, distribution quality control, distribution defect reduction activities, as shown in the flow chart in the following figure.

Figure 1-12. Semiconductor Device Distribution Flow

1.13.1 Packaging design control

In order to maintain semiconductor device quality under stress in the logistics system (transportation, storage, warehousing operations, etc.), it is important to design the proper storage cases made up of trays, magazines, tape, etc. and packaging materials such as packing boxes.

The storage case in particular must serve the role of protecting the device in the logistics stage while at the same time serve as a jig when the customer is installing the device. To aid in this task, various types of standardization activities are being conducted in Japan, centered around the JEITA (Japan Electronics and Information Technology Industries Association). In addition to taking part in these standardization activities, Compound Semiconductor Devices Division has a design policy that requires all designs to comply with JEITA standards, IEC standards, and other relevant industrial and international standards. In package design, Compound Semiconductor Devices Division thoroughly analyzes previous cases of abnormalities as it seeks to reduce the volume of packing materials while promoting the reuse and recycling of all such materials.
1.13.2 Logistics quality control

Quality of semiconductor devices while in logistics is influenced by storage control, the work environment related to shipping, transportation control, etc. If control in these processes is not adequate, there is a possibility that the packaging of products which require moisture-proof packages will be damaged, and soldering abnormalities will occur from rust, or the products will be destroyed by static electricity, or the leads will become abnormal due to mechanical stress, etc. For this reason, the controls shown in Table 1-2 are implemented in each process.

<table>
<thead>
<tr>
<th>Category</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage</td>
<td>• Temperature, humidity, atmosphere, mechanical stress, direct sunlight</td>
</tr>
<tr>
<td></td>
<td>and static electricity in the storage place</td>
</tr>
<tr>
<td></td>
<td>• Control of products that are rusting due to moisture, etc. or that have</td>
</tr>
<tr>
<td></td>
<td>been stored for long periods of time</td>
</tr>
<tr>
<td>Work</td>
<td>• Temperature, humidity, dust and other atmospheric conditions</td>
</tr>
<tr>
<td></td>
<td>• Design control, standard operations</td>
</tr>
<tr>
<td>Transportation</td>
<td>• Strict adherence to handling instruction marks (this side up,</td>
</tr>
<tr>
<td></td>
<td>cautions about the number of stacking tiers, etc.)</td>
</tr>
<tr>
<td></td>
<td>• Direct sunlight, vibration, etc.</td>
</tr>
</tbody>
</table>

1.13.3 Logistics defect reduction

The defects detected in the logistics stage which is shown in Figure 1-12 are defined as “Logistics Defects” and representative modes are shown in Table 1-3.

<table>
<thead>
<tr>
<th>Defect Mode</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Indication defect</td>
<td>If the contents written on the package differ from the specification and from the product itself.</td>
</tr>
<tr>
<td>Differences in product</td>
<td>If the product name, standards, and lot differ from the specifications.</td>
</tr>
<tr>
<td>Quantity mismatching</td>
<td>If there are more, or fewer of the product than specified or than indicated on the package.</td>
</tr>
<tr>
<td>Damage</td>
<td>If the leads on the product are bent, or the package is damaged.</td>
</tr>
</tbody>
</table>

Logistics defects are recorded on standardized forms based on standards for handling logistics defects. These forms include descriptions of defects, their causes, preliminary or permanent corrective measures that are implemented, as well as plans for preventive measures, etc. The contents of logistics defects recorded in the ledger are also subjected to analysis through statistical methods and defect reduction activities are implemented for major points.
1.14 Process Information Control and Customer Complaints Response System

1.14.1 Process information control system

In the effort to meet the manifold requirements of customers and to constantly develop higher performance semiconductor devices, the manufacturing line has become a multiple product line where new products are frequently being introduced. In order to successfully carry out efficient production on such a line, we are providing an in-process information control system.

The process information control system carries out the following types of control.

1. Operating conditions control and instructions

All operating conditions specified by the engineering department are controlled in real time and equipment is set automatically to the proper operating conditions. Through this, automatic operation becomes possible. For off-line equipment, operating conditions are displayed.

2. Collection of operating information

Operating report data for all the equipment are gathered. In this way, the progress of all lots and the operating conditions of the equipment can be ascertained, and production control, equipment control, and conveyance instructions can be carried out efficiently.

3. Storage of lot history

The operating history of all lots and process inspection data are stored as the lot history. This information can be analyzed as a data base and utilized in process control and process improvements.

Figure 1-13 shows the above in concrete form.

Figure 1-13. Process Information Control System
1.14.2 Customer complaints response

(1) Complaints analysis flow
If a complaint is made by a customer, the cause of the defect is immediately investigated and the result of the investigation is conveyed to the related department(s) as necessary to prevent recurrence. If the cause of the defect cannot be determined, the customer is requested to confirm the symptom of the defect again so that the cause can be investigated.
Figure 1-14 shows the complaints analysis flow.
For complaints processing, accurate information on the defect from the customer is indispensable.

Example) Nature of defect, process where defect occurred, status of electrical, mechanical, and/or thermal stress, lot dependency, recurrence, rate of occurrence, condition of peripheral components, usage, bending of leads, and package indication (such as a difference in model and mixing different models)
The product in which a defect occurred should be returned to Compound Semiconductor Devices Division with the condition of occurrence of the defect kept unchanged. In addition, consideration should be taken so that no external stress is applied to the product in question while it is transported.

(2) Defect information control system
Compound Semiconductor Devices Division registers information on defects reported by customers to its defect quality information system, so that necessary information can be retrieved and used online, in order to prevent recurrence.
Figure 1-14. Complaints Analysis Flow

Customer

Request for investigation

Sales department

Complaints investigation analysis request

Reliability and Quality Control Department

Complaint investigation and analysis, Receiving procedures (checking the product)

Visual inspection (including packaging, indications)

Electrical Specifications test

Defective, failure mode classification

Product analysis

Investigation of the cause

Corrective measures (horizontal development if necessary)

Checking the results of corrective measures

Permanent countermeasures (recurrence prevention)

Manufacturing Company

Preparation of a report

Report

Reception of report

Sending the report
1.14.3 Collection of reliability data and servicing

Compound Semiconductor Devices Division examines the reliability test data of the product and fundamental data of the parts and materials in the development and design stages of a new product, to perform quality and reliability designing. Data of a new product, such as approval test data and periodically reliability check test, are obtained to predict the market failure rate and to maintain and improve product quality.

In addition, Compound Semiconductor Devices Division also has a system that can supply the following data necessary for product approval and acceptance inspection by the customer.

- Periodically reliability test (monitoring) data of each product family (period units)
- New product approval test data (product units)
- Approval data when product is changed in any way

1.15 Quality Records

Records concerning quality, such as design, production, and delivery records, are stored in a specific way. For example, the main documents concerning design, such as design standards, design specifications, and design review reports, are stored for 12 years.

The major manufacturing process records, lot management records, and electrical test data are stored for more than 5 years.

An example of the records kept in storage is shown in Table 1-4.

<table>
<thead>
<tr>
<th>Classification</th>
<th>Documents Stored</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design records</td>
<td>Design standards, specifications, drawings, design investigation reports, records of changes</td>
</tr>
<tr>
<td>Manufacturing records</td>
<td>Manufacturing history, process check records, equipment check records</td>
</tr>
<tr>
<td>Inspection records</td>
<td>Inspection results</td>
</tr>
</tbody>
</table>
1.16 Statistical Techniques

1.16.1 Outline

In order to build stable quality into products at the design and manufacturing stages, Compound Semiconductor Devices Division utilizes statistical techniques at each stage.

In the design stage, together with fluctuations in the manufacturing process, such as film thickness and dimensions, being taken into consideration, design (robust design) is carried out with product characteristics which cannot be easily influenced by fluctuations within the process.

In the manufacturing stage, control charts are applied in the important processes and conditions are monitored at all times so that variations are within the correct range. Also, through control of the process capacity index (Cp, Cpk), efforts are being made to further reduce variations. At Compound Semiconductor Devices Division, process data and equipment data in particular are controlled by computer and through statistical processing, automation of statistical process control (SPC) is proceeding. In this way, it is becoming possible to exercise even more minute control. Although equipment model sorting and scatter diagrams are often used as part of failure analysis, we are also promoting the use of computers to facilitate analysis by entering process data in computers.

Also, in order to link statistical techniques to effective improvements, efforts are being made to make statistical techniques common knowledge by incorporating them into Compound Semiconductor Devices Division’s educational curriculum, with operators, engineers and management undergoing education at different levels.

1.16.2 SPC (Statistical Process Control)

(1) Process control through control charts

Manufacturing process control data are controlled by check sheets, graphs and control charts, etc., but for important processes, the stability of process variations is checked using control charts. Control charts are made by estimating control limits which show a range for normally generated data from the variation \( \sigma \) of process data within a predetermined range (mean \( \pm 3\sigma \)), and entering them on a chart designed for recording of measured data. If some factor which causes the process variations to deviate from normal occurs, data are outputs which go beyond the control limit lines, so these charts are effective in detecting process variations rapidly. Not only deviations from the control limit, but also tendencies of data to rise or fall are a means of detecting process fluctuations.

(2) Process capacity index

The degree of stability of a process can be determined from the process data for a given internal and standard values. This is called the process capacity index (Cp, Cpk), and is determined using the following formulas.

\[
C_p = \frac{(\text{Standard upper limit} - \text{Standard lower limit})}{6\sigma}
\]

(Process capacity index when taking skewing of data with respect to the standard center value (mean value) into account)

\[
C_{pk} = \frac{|\text{Nearest standard limit to mean} - \text{mean}|}{3\sigma}
\]

At Compound Semiconductor Devices Division, the process capacity index is determined periodically and efforts are made to improve process variations.
A Compound Semiconductor Devices Division promotes the introduction of QWACS (Quality early Warning Alarm Control System) or similar systems that enable the automatic generation of control charts and sensor alarms. One such QWACS system is outlined in Figure 1-15.

Figure 1-15 shows an outline of the QWACS.

Figure 1-15. QWACS System
(b) Process improvement activities through QWACS

Through QWACS, process data are monitored constantly and minute process control can be carried out. Since data are being monitored at all times, tendencies to abnormality are detected early and product abnormalities can be prevented before they occur. When an alarm is generated, the appropriate measures are taken by the engineering department or the manufacturing department, and prevention of recurrence is carried out. Also, the process capacity index is checked periodically and the total conditions are ascertained in addition to activities being conducted to further improve the important processes. Figure 1-16 shows an outline of improvement activities.

Figure 1-16. Outline of Process Improvement Activities Through QWACS
1.17 Tackling Environment Management

1.17.1 Outline

Compound Semiconductor Devices Division aims to become a green partner that creates value together with the customer, using two main pillars, ecological products and ecological factories, to satisfy the customers’ needs.

(1) Basic environmental protection policy

The 21st century is called the century of environment. This is because, we, human beings, must tackle the ecological problems that have surfaced at the end of the 20th century in this century. Companies must consider protection of the environment as an important task of management, and perform business management taking responsibility as global citizens. Therefore, Compound Semiconductor Devices Division has promoted environment management activities, so that its business activities include activities to protect and maintain the environment. Compound Semiconductor Devices Division intends to become a green partner that can satisfy the environmental needs of its customers, and to contribute to environmental protection through ecological product activities that reduce the environmental impact of products, and ecological factory activities that lowers the environmental impact of manufacturing plants.

Figure 1-17. Environmental Protection Activities of Compound Semiconductor Devices Division
1.17.2 Environmental management system

(1) Environmental policy

Philosophy
We will contribute to conservation of the global environment in the course of our activities within the semiconductor industry.

Activity Principles
1. We will incorporate environmental considerations into all stages of our product life cycle, including development, procurement, production, sale, use and disposal.
2. We will strive to prevent pollution as well as minimize impacts on the environment caused by chemical substances.
3. Our environmental management efforts will involve compliance with all environmental laws and regulations and other demands to which we have given our consent as well as establishment of own voluntary environmental standards.
4. We will educate all employees in environmental management and foster awareness of environment, safety and health.
5. We will regularly review our environmental management system and continually improve environmental activities.

(2) Promotion system

Compound Semiconductor Devices Division, a member of the NEC Electronics, has the following two councils and sub-council: (1) The "Eco-Products Promotion Council," which is organized by NEC Electronics and is composed mainly of development and design groups, (2) the "Eco-Production Promotion Council," which is composed mainly of groups of divisions engaging in production that may be environmentally burdensome, and (3) the sub-council, "Chemical Substance Working Group." These councils and sub-council promote various types of "Eco-Product Activities" and "Eco-Factory Activities."
To deal with pressing key issues, each promotion council has various specialized promotion sub-councils. At present, the Eco-Products Promotion Council oversees the Green Products Promotion Sub-Group and the Customer Response Operations Sub-Group, and the Eco-Production Promotion Council oversees an Energy Working Group, PFC Working Group, and Environmental Safety Working Group.
Our in-house organization also includes a Preliminary Evaluation Sub-council (which evaluates new chemicals and plant equipment before they are introduced, performs preliminary studies of equipment disposal methods, and carries out product assessments). These sub-councils perform various checks and activities and help determine policies in their respective fields of new equipment and Eco-product activities.

1.17.3 Basic policy for Pb-free production

(1) We will contribute to global environmental conservation through our active promotion of lead-free.

(2) We have completed development of lead elimination technologies for semiconductor products and are now able to offer lead-free versions of all new products.

(3) One of our environmental goals is to totally eliminate lead from all of our products, and we are smoothly switching over to lead-free products with the full support and understanding of our customers.
### CHAPTER 2 RELIABILITY OF SEMICONDUCTORS

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</table>
CHAPTER 2 RELIABILITY OF SEMICONDUCTORS

2.1 Approach to Reliability

2.1.1 Definition of reliability

According to the Japanese Industrial Standards (JIS Z 8115, Glossary of terms used in reliability), reliability is defined as characteristics that enable an item to perform its required functions under the stipulated conditions and for the stipulated time period. In other words, reliability resides in characteristics that enable a product to operate without malfunctions for the intended use period, which refers to a product's quality over time.

Quantifiable yardsticks such as the reliability rate, failure rate, and mean time to failure (MTTF) are used to measure reliability.
2.1.2 Reliability of semiconductors

To evaluate the reliability of an electronic system, reliability information on the components used in that system is important. Failure rates are often used as an index for reliability. A failure rate indicates how often a failure occurs per unit time, and failure-rate values generally change over time as shown in Figure 2-1.

Each failure area in this figure is explained below.

Figure 2-1. Time-Related Changes in Failure Rate

- **Early failure stage:** During this stage, failures occur at a high rate following the initial operation of semiconductor devices. They occur very soon and thus the failure rate declines rapidly over time. This is because the potential failures that could not be removed through a selective process are included and surface in a short time if a stress such as temperature or voltage is applied after use of the device is started. In the case of semiconductors, these failures are usually due to defects that could not be removed during production, such as micro dust collecting on the wafer, or to material defects.

- **Random failure stage:** When early failures are eliminated, the failure rate drops to an extremely low value. However, there is always the possibility of a potential failure accidentally occurring after a long time. Consequently, the failure rate never decreases to zero. It is almost constant because failures occur sporadically.

- **Wear-out failure stage:** During this stage, failures occur with increasing frequency over time and are caused by age-related wear and fatigue. In the case of a semiconductor device, electronic migration or oxide film destruction (TDDB) may occur (see **CHAPTER 3 FAILURE MODES AND MECHANISMS**).

The failure rate is generally expressed in \((\text{fit} = 10^{-9}/\text{h})\). This indicates the number of failures per unit time. In general, the mean failure rate of a semiconductor device per unit time is calculated with the following expression.

\[
\text{Mean failure rate} = \frac{\text{Total number of failures in given period}}{\text{Number of base devices} \times \text{Operation time}}
\]

According to this expression, 1 (fit) is expressed as follows.

\[
1 \text{ (fit)} = \frac{1 \times 10^9}{\text{Number of bases: 100000} \times \text{Operation time: 10000 hours}}
\]

In other words, 1 (fit) is equivalent to a failure of one device per 100,000 devices operated for 10,000 hours.
2.1.3 Activities to improve reliability

As a manufacturer of electronic components, it is essential that Compound Semiconductor Devices Division perform a cycle of activities to improve reliability. This cycle is illustrated in Figure 2-2.

(1) Understanding market needs, customers’ reliability requirements, and use conditions

When developing new products, it is important to understand market needs, customer’s requirements and use conditions, information about the use environment, etc. An understanding of such information should be reflected in product designs and manufacturing processes. Specific information may include the customer’s reliability requirements, use conditions such as the ambient temperature, humidity, and power supply voltage, and environmental conditions such as vibration, static electricity, and application of overvoltage. Information from customer complaints can also be used to gain insights into market needs.

(2) Creation of reliability

Design for reliability is performed to ensure that an understanding of needs (market needs, customer needs, etc.) is reflected in the design of products. Key elements include parameter design, quality and function deployment, FMEA, and FTA methods, etc.
(3) **Reliability evaluation**

Design reviews are performed to confirm and evaluate the suitability of product designs. They verify whether or not a design complies with the relevant design standards, whether or not the selection standards and the evaluation are appropriate when using new materials or new processes. The reliability evaluation process also includes collective measures against abnormalities. In addition, the design review must also confirm whether or not the expected level of reliability has been built into prototype samples. Usually, accelerated tests are used in reliability testing to reduce evaluation time and costs. Acceleration conditions in which hypothesized failure matches to the market results should be determined.

(4) **Analysis of evaluation results**

Failure analysis methods are used to look for causes of failures that occur during reliability testing or that are described in complaint reports. Here, the objective is to provide feedback to the design and screening processes by determining which mechanisms cause problems in which mode. Also, the reliability test results can be used with statistical methods to estimate a product's age-related quality (failure rate, etc.).

(5) **Feedback from results**

To prevent failures, the product's design and manufacturing processes must be reviewed and revised. If revisions need to be extended to other product as well, the revisions must be worked into the standards (design standards, manufacturing process standards, etc.) that apply to those products.

The above steps are cycled through in order to bring ever higher levels of reliability to product designs.

This chapter explores some of the above-mentioned topics that are important for verifying and improving reliability. Specifically, reliability testing, failure modes and failure analysis (including failure analysis devices) are described in this chapter.
2.2 Reliability Testing

2.2.1 What is reliability testing?

Customers naturally expect semiconductor devices to perform the required functions from the moment they are first used, and they also expect the devices to function without failure throughout the expected use period. This brings us back to the above-mentioned definition of reliability as characteristics that enable an item to perform its required functions under the stipulated conditions and for the stipulated time period.

According to JIS Z 8115 (Glossary of terms used in reliability), reliability testing is defined as a general term referring to tests that determine reliability and tests that evaluate the suitability of reliability. In other words, reliability testing is intended to confirm whether or not reliability required by customers are present in semiconductor devices.

2.2.2 Reliability test methods

(1) General

The objective of reliability testing is to confirm a semiconductor device's fault-free operation and to estimate its useful life by exposing the device to accelerated or marginal stress based on the amount of stress (thermal stress, mechanical stress, electrical stress, etc.) that the device is estimated to undergo during manufacture, shipping, and use.

To achieve this objective, it is important even as early as the semiconductor device planning stage to fully understand customer needs and the range of market applications so as to establish appropriate quality and reliability levels, which can be confirmed via appropriate reliability tests.

Reliability tests are performed under various stress conditions that are based on hypothesized stress conditions during manufacture, shipping, and use, and various semiconductor device testing methods have been standardized, such as in the Japanese Industrial Standards (JIS), the Japan Electronics and Information Technology Industries Association (JEITA) Standards, Military Specifications and Standards (MIL), and the International Electrotechnical Commission (IEC) Standards.

The stress received by semiconductor devices includes mechanical stress such as shock or vibration, thermal stress such as soldering temperature or ambient temperature, and electrical stress such as electrical currents or voltages. The tests that verify how resistant devices are to such stress are broadly divided into environmental tests and endurance tests.

Table 2-1 lists some typical categories of reliability tests conducted at Compound Semiconductor Devices Division.
## Table 2-1. Example of Reliability Test Categories for Semiconductor Devices

<table>
<thead>
<tr>
<th>Test Category</th>
<th>Relevant Standards</th>
<th>Test Method and Test Conditions</th>
<th>Examples of Detectable Failure Mechanisms</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Environmental tests</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistance to soldering heat</td>
<td>ED-4701 301 302</td>
<td>260 ±5°C for 10 seconds</td>
<td>Package crack Chip crack Bonding failing off</td>
</tr>
<tr>
<td>Temperature cycle</td>
<td>MIL-STD-883 105 1010 Condition C</td>
<td>One cycle: test at below minimum temperature for 30 minutes, then test at above maximum temperature for 30 minutes. 10 cycles</td>
<td></td>
</tr>
<tr>
<td>Thermal shock</td>
<td>MIL-STD-883 307 1011 Condition C</td>
<td>100°C for at least 5 minutes 0°C for at least 5 minutes 15 cycles</td>
<td></td>
</tr>
<tr>
<td>Variable frequency vibration</td>
<td>MIL-STD-883 403 2007 Condition A</td>
<td>Peak 20 G, 20 to 2,000 Hz 4 times for 4 minutes in each direction (X, Y, and Z)</td>
<td>Package crack Chip crack Bonding failing off</td>
</tr>
<tr>
<td>Shock</td>
<td>MIL-STD-883 404 2002 Condition B</td>
<td>1,500 G 3 times for 0.5 ms in each direction (X, Y, and Z)</td>
<td></td>
</tr>
<tr>
<td>Constant acceleration</td>
<td>MIL-STD-883 405 2001 Condition D</td>
<td>20,000 G 1 time for 1 minute in each direction (X, Y, and Z)</td>
<td></td>
</tr>
<tr>
<td>Solderability</td>
<td>MIL-STD-883 303 2003</td>
<td>215 ±5°C or 245 ±5°C for five seconds, with flux</td>
<td>Package crack</td>
</tr>
<tr>
<td>Terminal strength (bending)</td>
<td>MIL-STD-883 – 2004 Condition B2</td>
<td>Three times for randomly selected pins, using rated weight and bending to 90 (±5) degrees</td>
<td>Package crack</td>
</tr>
<tr>
<td><strong>Endurance tests</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High temperature storage</td>
<td>MIL-STD-883 201 1008</td>
<td>Test at above maximum temperature for at least 1,000 hours</td>
<td>Intermetallic compound Stress migration</td>
</tr>
<tr>
<td>Continuous operation or high temperature bias</td>
<td>MIL-STD-883 101 1005</td>
<td>T&lt;sub&gt;x&lt;/sub&gt;: 125°C or above for at least 1,000 hours Type of test and load conditions are determined by test.</td>
<td>Ion contamination Oxide layer damage Broken junctions</td>
</tr>
<tr>
<td>Intermittent operation</td>
<td>MIL-STD-883 106 1006</td>
<td>Access via continuous operation and ON/OFF cycles are determined by test.</td>
<td></td>
</tr>
<tr>
<td>Humidity resistance</td>
<td>MIL-STD-883 102 –</td>
<td>T&lt;sub&gt;x&lt;/sub&gt;: 85°C, RH: 85% for at least 1,000 hours When there are applied voltage and load conditions, they are determined by test.</td>
<td>Aluminum corrosion</td>
</tr>
<tr>
<td>Pressure cooker test (PCT)</td>
<td>MIL-STD-883 – –</td>
<td>Exposure to hot vapor (125°C, RH 100%) having 2.3 barometric pressure for at least 96 hours</td>
<td>Aluminum corrosion</td>
</tr>
<tr>
<td>Temperature cycle</td>
<td>MIL-STD-883 105 1010</td>
<td>One cycle: test at below minimum temperature for 30 minutes, then test at above maximum temperature for 30 minutes. 100 cycles or more</td>
<td>Package crack Chip crack Aluminum slide</td>
</tr>
</tbody>
</table>

**Notes**

1. Applicable for hermetically sealed packages
2. Select either continuous operation or intermittent operation according to device relevant specification.
3. Applicable for mold-resin type packages
4. Applicable only for certification testing
Environmental tests

These environmental tests use simulations of models wherein a semiconductor device that is undergoing stress fails when limit values are exceeded. Environmental tests are broadly divided into thermal environmental tests and mechanical environmental tests.

<1> Thermal environmental tests
The objective of thermal environmental tests is to confirm a mounted semiconductor device’s resistance to the thermal stress conditions it is under during its use period. Using thermal stress equivalent that applied during solder mounting, the samples are tested under a series of thermal variation stress conditions. The maximum rated soldering temperature is used during soldering.

<2> Mechanical environmental tests
The objective of mechanical environmental tests is to confirm a manufactured semiconductor device’s resistance to the mechanical stress conditions it is under during shipping, mounting, and use. The amount of stress applied is estimated as being greater than the amount actually experienced during shipping, mounting, and use.

Endurance tests

Endurance tests use simulations of models wherein a semiconductor device is exposed to stress conditions that are below the limit values but that are applied over time to test for age-related failures. Semiconductor devices generally have a long useful life, which makes it very difficult to test endurance under ordinary use conditions. Therefore, when stress that exceeds the rated value is applied to a semiconductor device, age-related deterioration is accelerated so that the device’s useful life can be measured in a relatively short time. This type of test method is called accelerated life testing.

2.2.3 Accelerated life testing

(1) General
Accelerated life testing is used to predict the device’s useful life and failure rate in a short testing period. Accelerated life testing exposes a semiconductor device to stress conditions that are harsher than during actual use, the speed of reactions to failure events is also accelerated, which speeds up aged-related deterioration and shortens the testing period. However, correct life estimations cannot be made unless selected test methods have failure modes that are similar to the failure modes under actual use conditions.

(2) Acceleration using thermal stress
In many cases, the Arrhenius model is used to represent physical and chemical events related to deterioration of semiconductor devices. The Arrhenius model is a basic chemical reaction model for temperature-dependent failures, and in this case it is applied to estimate the useful life of semiconductor devices which are subjected accelerated life tests that use thermal stress.

Life (L) is expressed as follows in the Arrhenius model.

\[ L = A \cdot \exp \left( \frac{E_a}{kT} \right) \]

Where,
- L: Life
- A: Constant
- E_a: Activation energy [eV]
- k: Boltzmann’s constant \((8.62 \times 10^{-5} \text{ eV/K})\)
- T: Absolute temperature [K]
This equation expresses the relation between temperature and product life, so that if the failure mode is the same, the relationship between life (ln L) and temperature (1/T) values obtained from life testing will be as shown in Figure 2-3, which enables product life under actual temperature (T0) to be estimated. The type of diagram shown in the figure is called an Arrhenius plot. The slanted line in Figure 2-3 represents the activation energy (Ea).

Figures 2-4 and 2-5 show changes over time that occur during accelerated life testing. As can be seen in Figure 2-4, changes in characteristics occur at temperature values of 337°C, 295°C, and 259°C. The graph of changes over time indicates a rapid rate of acceleration. Figure 2-5 shows an Arrhenius plot of the test results. The angle of the line indicates an activation energy (Ea) of approximately 1.5 eV. This activation energy and the temperature-dependent changes over time during testing can be used to estimate the changes that will occur under actual use environment temperatures.

**Figure 2-3. Arrhenius Plot (Relation Between Life and Temperature)**

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Rate of change (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>259°C</td>
<td>50</td>
</tr>
<tr>
<td>295°C</td>
<td>40</td>
</tr>
<tr>
<td>337°C</td>
<td>30</td>
</tr>
<tr>
<td>259°C</td>
<td>20</td>
</tr>
<tr>
<td>295°C</td>
<td>10</td>
</tr>
<tr>
<td>337°C</td>
<td>0</td>
</tr>
<tr>
<td>259°C</td>
<td>-10</td>
</tr>
<tr>
<td>295°C</td>
<td>-20</td>
</tr>
<tr>
<td>337°C</td>
<td>-30</td>
</tr>
<tr>
<td>259°C</td>
<td>-40</td>
</tr>
<tr>
<td>295°C</td>
<td>-50</td>
</tr>
<tr>
<td>337°C</td>
<td>-60</td>
</tr>
</tbody>
</table>

**Figure 2-4. Graph of Age-Related Changes**
(3) **Failure modes based on higher temperatures**

Failures that ordinarily occur in semiconductor devices can be accelerated by higher temperatures. However, even when the failure modes are the same, there are various failure mechanisms that can occur. Since the reaction speed varies among different failure mechanisms, the activation energy also varies. Therefore, the failure mechanism can be considered an analog of the activation energy, which enables life estimations to be made.

Table 2-2 lists typical failure modes, failure mechanisms, and activation energy values related to higher temperatures in semiconductor devices.

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Failure Mechanism</th>
<th>Activation Energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vt variation</td>
<td>Ion contamination</td>
<td>1.0 to 1.4</td>
</tr>
<tr>
<td></td>
<td>Slow trapping</td>
<td>1.0 to 1.5</td>
</tr>
<tr>
<td>Short</td>
<td>Oxide layer damage</td>
<td>0.3</td>
</tr>
<tr>
<td>Open</td>
<td>Electromigration in wiring</td>
<td>0.5 to 1.0</td>
</tr>
<tr>
<td></td>
<td>Au-Al intermetallic compound</td>
<td>0.8 to 1.0</td>
</tr>
<tr>
<td></td>
<td>Corrosion of Al wiring</td>
<td>0.5 to 1.0</td>
</tr>
<tr>
<td>Increased leakage current</td>
<td>Generation of inversion layer</td>
<td>0.5 to 1.0</td>
</tr>
</tbody>
</table>
(4) **Acceleration based on humidity**

Recently, mold plastic semiconductor devices have come into wide use. The reliability of mold resin type semiconductor devices depends greatly on the device’s humidity resistance, and various test methods are used to provide an early evaluation of reliability. Typical testing methods are described in Table 2-3. At Compound Semiconductor Devices Division, high temperature/high humidity bias testing (or storage testing) and pressure cooker testing (PCT) are performed to check humidity resistance.

Humidity resistance testing is prone, however, to problems such as variation in reproducibility and failure modes that differ from actual use results, and consequently extra caution is required when implementing humidity resistance tests.

In addition, recent semiconductor devices are mainly surface mount devices (SMDs), which are becoming smaller, thinner. For these devices, thermal stress during mounting and moisture absorption in resin during storage are two factors that cannot be ignored. To correctly simulate actual use, mounting stress is applied as shown in Figure 2-6, in a preprocess that is part of humidity resistance testing.

**Table 2-3. Main Moisture Resistance Testing Methods**

<table>
<thead>
<tr>
<th>Testing Method</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>High temperature, high humidity storage test (HHT)</td>
<td>85°C/85% RH</td>
</tr>
<tr>
<td>Pressure cooker test (PCT)</td>
<td>125°C/100% RH</td>
</tr>
<tr>
<td>High temperature, high humidity bias test (HHBT)</td>
<td>85°C/85% RH</td>
</tr>
<tr>
<td></td>
<td>Bias is applied</td>
</tr>
<tr>
<td>Unsaturated pressure cooker bias test with bias</td>
<td>130°C/85% RH</td>
</tr>
<tr>
<td></td>
<td>Bias is applied</td>
</tr>
</tbody>
</table>

**Figure 2-6. Examples of Simulation of Soldering Heat**

```
Dry 125°C

Moisture absorption 30°C/70%RH or 85°C/85%RH

Infrared reflow 260°C, 1 to 3 times
```
(5) Screening

Screening is implemented to eliminate early failures. In one type of screening, a suitable amount of stress (not enough to wear down or damage a device that has no latent defects) is intentionally applied to products to wear down latent defects so that they can be detected and removed by appropriate tests performed afterward. In another type of screening, defective products are detected and removed at a suitable stage during manufacturing and without having to apply stress. These screening concepts are described in Figure 2-7.

When selecting an appropriate type of screening for a product, a great deal of consideration must be given to the product’s applications, the required quality level, as well as the product’s design, structure, and fabrication method. In addition, the screening process must not have an adverse impact on nondefective products. Table 2-4 lists some typical screening methods being used today. Suitable screening methods are selected and applied for the actual products based on the required quality level and/or required specifications.

![Figure 2-7. Variation in Quality Level Due to Screening](image)

<table>
<thead>
<tr>
<th>Type</th>
<th>Screening Method</th>
<th>Expected Failure Removal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-stress methods</td>
<td>Visual inspection before sealing</td>
<td>Die surface defects, bonding wire defects, etc.</td>
</tr>
<tr>
<td></td>
<td>Visual inspection after sealing</td>
<td>Package surface defects, damage, etc.</td>
</tr>
<tr>
<td></td>
<td>X-ray fluoroscopy</td>
<td>Bonding wire distortion, die bond and eutectic alloy defects, etc.</td>
</tr>
<tr>
<td>Thermal stress methods</td>
<td>Temperature cycle</td>
<td>Die bond, package defects, hermetic sealing defects, etc.</td>
</tr>
<tr>
<td></td>
<td>Thermal shock</td>
<td>Same as above</td>
</tr>
<tr>
<td></td>
<td>Low-temperature test</td>
<td>Effect of hot carrier, variation in electrical characteristics, etc.</td>
</tr>
<tr>
<td>Mechanical stress methods</td>
<td>Drop impact</td>
<td>Die bond, bonding wire and package defects, etc.</td>
</tr>
<tr>
<td></td>
<td>Constant acceleration</td>
<td>Same as above</td>
</tr>
<tr>
<td></td>
<td>PIND</td>
<td>Foreign particles in cavities within packages</td>
</tr>
<tr>
<td>Electrical stress methods</td>
<td>Burn-in</td>
<td>Defects inside the die, such as micro particles, dirt, and thin-film defects</td>
</tr>
<tr>
<td></td>
<td>Application of high voltage</td>
<td>Inadequate insulation layer, inadequate voltage resistance in circuit, etc.</td>
</tr>
</tbody>
</table>
2.3 Failure Rate Prediction Methods

2.3.1 Concept of failure rate

**Difference between failure rate and defect rate**

Where there are \( r \) defects in a population of \( n \) units, the defect rate is expressed as \( r/n \). The defect rate does not take time lapse into consideration, and indicates the ratio at which defects exist. In contrast, the failure rate indicates the rate at which failures occur per unit time, and varies over the time during which the device or system is operated. It is therefore an index intrinsically different from defect rate.

2.3.2 Failure rate prediction methods

(1) **Failure rate estimation method**

The failure rate of a general semiconductor device is considered to be about several to several 100 fit, which is lower than for other electronic components such as capacitors and switches. It is therefore difficult to actually measure the failure rate of a semiconductor device, but there are ways to accomplish this. If the failure rate of the same device is calculated by different prediction methods, however, an error of one to two digits may occur. It is therefore important not to judge the reliability of the device based on values alone, but to also give careful consideration to the prediction method(s).

(2) **Types and features of prediction**

Table 2-5 lists some typical failure rate prediction methods and their features.

<table>
<thead>
<tr>
<th>Method</th>
<th>Advantages</th>
<th>Caution Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimation based on life testing</td>
<td>Reliability test data can be used.</td>
<td>Amount of data is limited.</td>
</tr>
<tr>
<td></td>
<td>Data can be obtained under controlled conditions.</td>
<td>Failures often do not occur during the fixed time test period (resulting in poor estimation accuracy).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Caution is required concerning failure mode differences between tests and actual use.</td>
</tr>
<tr>
<td>Estimation based on market results</td>
<td>Raw data is obtained.</td>
<td>To get an accurate grasp of the data, information on the customer's use conditions and monitoring of time to failure are required.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This method is not suitable when the product is fabricated using a new process or in other cases where there are no previous market results.</td>
</tr>
<tr>
<td>Estimation based on prediction formula</td>
<td>Enables immediate estimations.</td>
<td>It is difficult to determine the prediction formula and the reliability factor coefficients.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A correlation must be made periodically between prediction formula results and life testing results and market results.</td>
</tr>
</tbody>
</table>
2.3.3 Prediction methods used at Compound Semiconductor Devices Division

(1) Failure rate prediction methods
At Compound Semiconductor Devices Division, the following methods are used to calculate failure rates. Generally, estimates are performed based on trends taken from life tests and also based on prediction formulas. How to estimate a failure rate using a typical life test is explained below.

[Failure rate estimation based on life testing]
Even though the product functions are specific to each product, if the process (design rule) is the same, the design quality can be considered as roughly equivalent. When life testing results for product models that use the same process are accumulated, it becomes possible to estimate their failure rate. This calculation is basically done using the following formula.

\[
\gamma_{b2} = \frac{P_2}{N_2 \times T_2 \times A} \times (60\% \text{ confidence level})
\]

where
- \(\gamma_{b2}\): Failure rate (based on life test results)
- \(P_2\): Total number of manufacturing defects
- \(N_2\): Total number of target devices shipped
- \(T_2\): Average operation hours (1920 h)
- \(A\): Rate of acceleration

(2) Calculation of failure rate for specific use conditions
The previous section describes failure rate calculation methods for semiconductor devices. When semiconductor devices are mounted onto a set and are operated, the failure rate must be adjusted to take the use environment into account.
To do this, the semiconductor device’s environmental conditions (such as temperature condition) are hypothesized and new failure rates are calculated for customers as shown in Table 2-6. The results of these calculations are used as the failure rates for actually used semiconductor devices.
The device’s failure rate \( \lambda \) is determined based on the device-specific basic failure rate \( \lambda_b \) and the use conditions. After considering the hypothetical use environment, the failure rate can be calculated via the following steps.

- Failure rate estimation formula \( \lambda \) (failure rate during random failure stage)

\[
\lambda = \lambda_b \times \pi_T \times \pi_V
\]

\( \pi_T \): Temperature parameter
\( \lambda_b \): Basic failure rate

1. \( \pi_T = \exp \left( \frac{11600 \times E_a}{273 + 55} \right) \times \left( \frac{1}{273 + T_A(j)} \right) \)

\( E_a \): Activation energy
\( T_A \): Ambient temperature during use (for IC)
\( T_j \): Junction temperature during use (for discrete device)

- \( \pi_V \): Power supply voltage parameter

\( \pi_V \) is applicable only for silicon transistors, FETs, and transistors with internal resistor. For products other than above, \( \pi_V = 1 \). (Calculation standard)

- Reliability level: 60%
- Basic temperature = 55°C
- Used under recommended conditions
2.3.4 Prediction method from MIL-HDBK-217

MIL-HDBK-217 (Department of Defense Military Handbook: Reliability Prediction of Electronic Equipment) was developed by the Pentagon with the assistance of the Department of the Army, various other Federal agencies, and industry representatives.

The purpose of creating the MIL-HDBK-217 handbook is to establish a uniform methodology for predicting the reliability of military electronic equipment and systems and to provide a common basis for reliability predictions performed at the acquisition program stage for military electronic equipment and systems. This handbook also establishes a common basis for comparing and evaluating reliability predictions of related or competing designs.

The data in the MIL-HDBK-217 handbook has been collected as field usage data for vast numbers of military electronic equipment that is purchased under MIL standards. Since compliance with MIL-HDBK-217 has been established by the Pentagon as a requirement in the military electronic equipment that it purchases, a safety coefficient must be fully taken into account for each factor. Consequently, the calculated failure rate for such devices tends to much greater than when using ordinary reliability prediction methods.

When a comparison is made between failure rates calculated using Compound Semiconductor Devices Division’s methods and failure rates calculated using MIL standard methods, the failure rate values for MIL are from 10 to 100 times greater than those for Compound Semiconductor Devices Division.
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### CHAPTER 3 FAILURE MODES AND MECHANISMS

#### 3.1 General

This chapter describes the principles of failure modes and failure mechanisms that occur in semiconductor devices. The relationships between the failure modes and failure causes are shown below.

Table 3-1. Relationships Between the Failure Modes and Failure Causes

<table>
<thead>
<tr>
<th>Failure Cause</th>
<th>Failure Mechanism</th>
<th>Failure Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Short</td>
</tr>
<tr>
<td>Bulk, board, diffusion, PN junction, isolation</td>
<td>Crystal defect</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Crack</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Surface contamination</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Junction degradation</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Impurity deposition</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Unadjustable mask</td>
<td>√</td>
</tr>
<tr>
<td>Gate oxide film</td>
<td>Moveable ion</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Interface level</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>TDDB</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Hot electron</td>
<td>√</td>
</tr>
<tr>
<td>Metallization, on-chip wiring, through hole,</td>
<td>Insufficient adhesion strength</td>
<td>√</td>
</tr>
<tr>
<td>contact</td>
<td>Ohmic contact</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Stage cut</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Uneven thickness</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Scar</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Corrosion</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Electromigration</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Al projection due to Al-Si alloy formation</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Al shift due to mold force</td>
<td>√</td>
</tr>
<tr>
<td>Passivation, surface protective film, inter-layer</td>
<td>Pin hole</td>
<td>√</td>
</tr>
<tr>
<td>insulation film</td>
<td>Crack</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Uneven thickness (step coverage block)</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Contamination</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Surface inversion</td>
<td>√</td>
</tr>
<tr>
<td>Die bonding</td>
<td>Chip peeling (uneven force, void)</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Thermal fatigue</td>
<td>√</td>
</tr>
<tr>
<td>Wire bonding</td>
<td>Substrate defect</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Removed bonding</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Intermetallic compound generation</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Damage and crack below bonding</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Bonding positional shift</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Loose wiring</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Line break</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Short between lines</td>
<td>√</td>
</tr>
<tr>
<td>Package, lead frame, resin, lead plating</td>
<td>Moisture (resin bulk)</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Moisture (resin interface)</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Impure ion of resin</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Surface contamination</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Hardening force</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Lead rust, oxidation</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Lead break</td>
<td>√</td>
</tr>
<tr>
<td>I/O pin</td>
<td>Party</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Static electricity</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Overvoltage</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Surge voltage</td>
<td>√</td>
</tr>
<tr>
<td></td>
<td>Latchup</td>
<td>√</td>
</tr>
</tbody>
</table>
3.2 Principal Failure Modes and Failure Mechanisms

3.2.1 Time dependent dielectric breakdown (TDDB)

(1) Dielectric withstand voltage defects in oxide layer
The causes of dielectric layer breakdowns include causes that stem from early defects and causes that reside within the dielectric layer materials. Ordinarily, the former type of causes tend to surface as early failures, and the latter type appear after a certain amount of time has elapsed. Consequently, the latter type of breakdown is referred to as time dependent dielectric breakdown (TDDB).

Figure 3-1 shows a histogram of dielectric withstand voltage distribution in thin oxide layers having relatively high quality. The distribution that approximates 10 MV/cm (mode C) indicates the dielectric withstand voltage (intrinsic withstand voltage) of a uniform oxide layer. The distribution that approximates 0 MV/cm (mode A) indicates that a non-uniform oxide layer was formed due to contamination during oxidation. The distribution that approximates 5 MV/cm (mode B) mainly indicates problems in the crystal quality of the silicon wafer surface. For example, when oxygen precipitates or nucleiues thereof are present in the crystals, defects are incorporated during formation of the oxide layer, which can lower the dielectric strength in some areas.

Figure 3-2 shows an oxide layer degradation model. When a strong electric field is applied to the oxide layer, a tunnel current flows (Fowler-Nordheim electron tunneling). The tunnel effect from the cathode causes electrons to be injected into the oxide layer, becoming “hot” electrons accelerated by the electric field. When these hot electrons collide with the crystal lattice, holes occur along with the electrons. These holes are mostly concentrated near the cathode, where a space charge is formed which gives rise to a positive feedback phenomenon that further accelerates the injection of electrons and contributes to dielectric breakdowns.
(2) Time dependent dielectric breakdowns (TDDBs) in oxide layer

Process miniaturization has resulted in increasingly thin oxide layers, which has increased the strength of electric fields within the oxide layers, so that when a voltage is continuously applied to the oxide layer, there is a rise in the ratio of oxide layer breakdowns that occur over time, which are known as time dependent dielectric breakdowns (TDDBs).

Figure 3-3 shows an example of TDDB characteristics. Although it is known that TDDBs are also dependent upon both electric field strength and temperature, their mechanisms are still unclear and remain a topic of ongoing research.

Currently, these types of breakdowns are being handled at fabrication processes by building oxide layers with fewer defects and by implementing appropriate burn-in procedures as part of the screening process so that randomly defective devices can be removed.

Figure 3-3. TDDB Characteristics
3.2.2 Injection of hot carriers

As advances in higher integration have been made in MOS ICs, a miniaturization trend has also occurred in MOS FET devices, which have now entered the submicron era. In the meantime, the supply voltage has changed from 5 V to 3.3 V, 2.5 V, and 1.8 V upon request from the system.

As a result, MOS FET devices have a stronger internal electric field which tends to generate highly charged electrons and holes (i.e., hot carriers). Various factors contribute to the generation of hot carriers, but the following two mechanisms are particularly significant.

(1) Hot carrier generation mechanism (using N-ch MOS FET as an example)

As shown in Figure 3-4, when electrons flow from a source toward a drain, before they reach the drain they are applied from an electric field vertical and are injected into the oxide layer when they exceed the potential barrier of the Si-SiO₂ interface. This type of hot carrier is called a channel hot carrier. Figure 3-5 also shows electrons that flow from a source toward a drain. In this case, a strong electric field near the drain causes ionization by collision or avalanche amplification, which also generates electron-hole pairs. At that point, some of the electrons and holes (hot carriers) are injected into the oxide layer. These hot carriers are called drain avalanche hot carriers. The conditions under which hot carriers are generated are determined by the conditions affecting the voltage applied to the MOS FET. The following is a brief description of how these hot carriers affect the MOS FET's electrical characteristics.

Figure 3-4. Channel Hot Carrier

![Channel Hot Carrier Diagram](image1)

Figure 3-5. Avalanche Hot Carrier

![Avalanche Hot Carrier Diagram](image2)

(2) Variation in MOS FET characteristics caused by hot carriers

The hot carriers that are injected into the gate's oxide layer can cause an interface level to occur at the Si-SiO₂ boundary or a trap level to occur in the gate oxide layer. As a result, variation occurs in the MOS FET’s threshold voltage and/or current characteristics. The direction of variation depends on whether the hot carriers are electrons, holes, or both. Given equal applied voltage conditions, the amount of variation in characteristics can be expressed using the following formula.

\[ \Delta P = A \times t^n \]

where \( \Delta P \): Variation in MOS FET characteristics

\( A, n \): Constant determined according to the MOS FET’s structure and applied stress voltage conditions

\( t \): Elapsed time (during application of stress)
Figure 3-6 illustrates the variation in an N-channel MOS FET’s threshold voltage when a constant current is applied.

**Figure 3-6. Variation in Threshold Voltage of N-channel MOS FET**

![Graph illustrating variation in threshold voltage](image)

Generally, the voltage applied to a MOS FET during operations changes between 0 V and the power supply voltage. Because the voltage is changing, hot carriers are not generated constantly and the variation in characteristics is less than when a constant voltage is applied. Furthermore, the device selects and deselects circuits, so that the cycle time and other factors also depend on the amount of variation. In MOS FETs fabricated via the same fabrication processes, variation in characteristics due to hot carriers is generally greater when the drain voltage (which in many cases corresponds to the power supply voltage) is greater or when the circuit is operating at a low temperature. Measures to prevent these hot carrier effects are described briefly below.

(3) **Measures to prevent hot carrier effects**

From the device perspective, a low-impurity layer can be established as a DDD\(^{Note 1}\) or LDD\(^{Note 2}\) structure to weaken the MOS FET’s internal electric field in order to reduce the amount of variation in MOS FET characteristics.

From the circuit design perspective, the circuit configuration can be designed to specifically control the voltage applied to MOS FETs during circuit operations as a way to prevent variation in device characteristics due to hot carrier effects.

**Notes**

1. **DDD**: Deeply Doped Drain
2. **LDD**: Lightly Doped Drain

---

\(^{Note 1}\): Deeply Doped Drain

\(^{Note 2}\): Lightly Doped Drain
3.2.3 Slow trap

When a voltage is applied to the gate electrode of a MOS transistor that is tested under a high temperature, a Vt shift is observed. This Vt shift depends greatly on the strength of the electric field that is applied to the gate electrode and is obvious when the voltage is negative. Figure 3-7 illustrates the temperature dependence of the Vt shift during BT testing of P-ch FETs, and Figure 3-8 illustrates the corresponding voltage dependence. Degradation of Vt was also observed over time when stress is applied.

As the trend of ultra-fine fabrication in semiconductor ICs continues, gate oxide layers are becoming thinner than ever and the strength of electric fields applied to gate electrodes is becoming greater. In CMOS devices, a negative voltage is applied to gate electrodes in P-channel transistors, which creates the risk that this type of Vt shift may occur.

The mechanisms of this Vt shift include the following.

1. When a carrier (hole) that is thermally excited exceeds the potential barrier of the interface, it becomes trapped near the interface. This phenomenon is called carrier trapping.

2. When a strong electric field is applied to the Si-H bonds that are present at the interface between Si and SiO₂, an interface level occurs and a positive charge is formed near the boundary.

This type of Vt shift phenomenon that is based on the movement of carriers at the boundary between the SiO₂ and Si as part of an injection-type shift is called a slow trapping phenomenon. This Vt shift is dependent on the package and the protective layer. The effect of external impurities is also recognized.

Figure 3-7. P-ch FET Vt Variation During BT Testing (Temperature Dependence)
Figure 3-8. P-ch FET Vt Variation During BT Testing (Voltage Dependence)

Reference

• Tsuneo Ajiki, editor, "Reliability Engineering for Semiconductor Devices," JUSE Press. Ltd. (Japanese version only)
3.2.4 Electromigration

In recent years, advances in large scale integration and fine process technology for semiconductor devices have increased wiring current density to the point where collisions between electrons and the metal atoms of the wiring material generate a mass transport phenomenon whereby momentum is gained in the electron flow direction, which leads to defects such as wire breakage, hillocks, whiskering, and shorting; these phenomena are known collectively as electromigration problems. Photo 3-1 shows an example of wire breakage that occurred during accelerated testing.

(1) Mechanisms behind electromigration phenomena

The metal wires that are used in semiconductor devices are formed by a sputtering process on dielectric layers that are sandwiched between other layers as part of a polycrystalline structure. The metal atoms, which gain momentum as they collide with electrons accumulate vacancies as they move along the grain boundary where diffusion is easiest. Eventually, if there are more output paths than input paths, voids occur as shown at point A in Figure 3-9. If there are more input paths than output paths, hillocks occur as shown at point B in the figure. If the wire size is less than the grain size, the crystal boundary forms a bamboo-like structure (see part <1> of Figure 3-10) that crosses the wiring, making grain boundary diffusion impossible and lengthening the time required to break the wiring when compared to wiring with a crystal boundary structure (see part <2> of Figure 3-10). Figure 3-11 shows an example of how MTF (median time to failure) is dependent on the wire size. Generally, the effect of electromigration on MTF can be expressed using Black’s empirical equation as follows.

\[ \text{MTF} = A j^{-n} \exp \left( \frac{E_a}{kT} \right) \]

Where
- A: Constants
- n: Activation energy [eV]
- k: Boltzmann’s constant (8.6159 \times 10^{-5} [eV/K])
- T: Absolute temperature [K]

In the above equation, the value of constant n is approximately 2, which indicates that the MTF is heavily dependent on the current density. A value ranging from 0.4 to 0.7 eV is obtained as the activation energy (Ea). Figure 3-12 shows an example of how MTF is dependent on temperature.
(2) Countermeasures to electromigration

The following are countermeasures that can be implemented to suppress electromigration-related defects.

<1> Enlarge the crystal grain width to reduce the grain boundary that serves as a diffusion path.

<2> Add elements such as copper or titanium to the wiring so reduce vacancies along the grain boundary and to suppress grain boundary diffusion using compound extraction.

<3> Make the structure of the wiring substrate more even to improve step coverage in sections with different levels, which prevents divergent electron flow and increased current density.

<4> Change the structure and shape of the dielectric layer and the cover layer to improve the strength of both, to improve the wiring fit, and to suppress formation of hillocks.

Photo 3-1. Example of Wire Breakage Due to Electromigration

Figure 3-9. Migration of Metal Atoms at Grain Boundary

Figure 3-10. Grain Boundary Structure of Wire
Figure 3-11. Wire Width Dependency of MTF

![Wire Width Dependency of MTF](image)

Figure 3-12. Temperature Dependency of MTF

![Temperature Dependency of MTF](image)

**Figure 3-11. Wire Width Dependency of MTF**

- **J = 2 \times 10^6 \text{ A/cm}^2**
- **T = 200°C**

**Figure 3-12. Temperature Dependency of MTF**

- **J = 2 \times 10^6 \text{ A/cm}^2**
- **E_a = 0.6 \text{ eV}**
3.2.5 Stress migration

Stress migration occurs when miniaturization of wiring causes a previously latent failure mechanism to become apparent, such as when aluminum wiring undergoes tensile stress due to different thermal expansion coefficients of the dielectric layer and the cover layer, and this thermal stress relaxation causes voids to occur due to thermal diffusion. Generally, there are two modes: (1) a low-temperature, long-term mode, where wire breakage occurs (such as in aging tests) during long-term storage at an ambient temperature of approximately 200°C; and (2) high-temperature, short-term mode, such as when voids occur during high-temperature thermal processing following film deposition.

(1) Low-temperature, long-term storage mode

During low-temperature, long-term storage mode, wedge-shaped voids occur or “bamboo boundary” (an aluminum grain boundary that appears like the lines between bamboo sections) appears. The highest failure rate when the ambient temperature is between 150°C and 200°C. Generally, these phenomena can be explained using a creep model of aluminum wire deformation when undergoing tensile stress. The creep rate can be expressed as the product of the stress term and the diffusion term. According to Arrhenius’s empirical rule, at high temperatures stress diminishes as the void diffusion rate increases, while at low temperatures stress increases as the diffusion rate slows, which indicates that there is a peak in temperature dependency. Photo 3-2 shows wire breakage that occurred due to a slit condition that developed during low-temperature, long-term storage mode.

The effect of stress migration on useful life depends greatly on the aluminum wire width and layer thickness, and is becoming a major problem in ICs.

Countermeasures that have been studied and proved to be effective include the following.

<1> Change the wire structure by adding a conductive layer having a high melting point (such as a TiN layer) onto the aluminum layer.

<2> Use dielectric and cover layers whose materials and structure feature low compressive stress in order to reduce tensile stress on the wiring.

<3> As is done for electromigration, add elements such as copper or titanium to the wiring to suppress grain boundary diffusion.

<4> Employ a wiring shape and a substrate shape that reduce stress concentration.
(2) **High-temperature, short-term storage mode**

In the high-temperature short-term storage mode, wedge-shaped voids occur during the cooling process following thermal processing, and it is understood that this phenomenon depends strongly on the type of dielectric layer. Countermeasures for this phenomenon include those listed above for low-temperature long-term storage mode, plus (and especially) suppressing thermal diffusion of metal atoms by lowering the temperature of thermal processing and speeding up cooling time.

The mechanisms of stress migration are still not fully understood. At present, various types of studies are being performed on stress analysis, void formation, TEM observation of growing processes, etc.

**Photo 3-2. Example of Stress Migration**
3.2.6 Aluminum corrosion

Currently, resin-seal type packages are widely used for semiconductor devices. When moisture from ambient air penetrates semiconductor devices in resin-seal type packages, failures can occur as a result of the following phenomena.

Degradation of electrical characteristics

Corrosion of aluminum wiring in chip

This section mainly describes aluminum corrosion phenomena.

(1) Paths for moisture permeation

There are two paths via which moisture can permeate resin-seal type devices.

<1> Permeation via the boundary between resin and leads
<2> Permeation via resin due to resin's moisture absorptivity

Figure 3-13 illustrates these two paths.

Path <1> is the main path, which exists due to the poor adhesion between the resin and lead frame. The amount of adhesion strength is determined by the materials used in the resin and lead frame, and this adhesion strength can be degraded by thermal stress that is applied during mounting.

Path <2> depends on the resin's moisture absorptivity. Moisture has been able to permeate packages via the resin more quickly in recent years due to thinner package designs.
(2) Aluminum corrosion mechanisms

Aluminum (Al) is a metal that is highly prone to electrochemical ionization and corrodes very easily. This electrochemical reaction is affected by the applied bias in that corrosion is greater at higher bias values and the corrosion mode differs depending on the polarity of the applied bias. This is because the electric fields that result from bias applications react with different ions depending on the polarity.

The ions associated with aluminum corrosion include chlorine ions and other halogen- or sodium-related ions. These ions are found in impurities in resin, on chip surfaces, and in flux used for mounting. Reaction formulas that express these corrosion factors are shown below.

<1> Reaction for anode
\[ Al + 4Cl^- \rightarrow AlCl_4^- + 3e^- \]
\[ AlCl_4^- + 3H_2O \rightarrow Al(OH)_3 + 3H^+ + 4Cl^- \]

<2> Reaction for cathode
\[ O_2 + 2H_2O + 4e^- \rightarrow 4(OH)^- \]
\[ Al + 3(OH)^- \rightarrow Al(OH)_3 + 3e^- \]
\[ 2Al + 6H_2O \rightarrow 2Al(OH)_3 + 6H^+ \]

Photo 3-3. Example of Aluminum Corrosion
(3) Estimated moisture resistance life

There are several main factors that must be considered to determine the moisture resistance life of a semiconductor.

<1> Moisture absorptivity of resin
<2> Adhesion strength between resin and semiconductor chip
<3> Amount of impurities in resin and/or semiconductor chip
<4> Strength of electric field
<5> Quality of chip protection layer
<6> Chip's internal circuit configuration and wiring materials

Due to complex combinations of effects created by these factors, there is no acceleration model that provides an overall description of these phenomena. However, the typical models are provided by the following life formulas. (A, B: Constants, t: Life)

<1> Reich – Hakim Model

\[ t = A \times \exp \left[-B \left(T_a \, ^\circ C + RH \, %\right)\right] \]

Example: B = 0.06

<2> Vapor – Pressure Model

\[ t = A \times V_p^{B} \]

Example: B = 1.82

<3> Eyring Model

\[ t = A \times \exp \left[ \frac{AE}{KT} + f \left(RH \, %\right) \right] \]

\[ f \left(RH \, %\right) = -4.4 \times 10^{-4} \times \left(RH \, %\right)^2 \]

OR

\[ f \left(RH \, %\right) = \frac{296}{(RH \, %)} \]

where

- \( T_a \): Ambient temperature [°C]
- \( T \): Absolute temperature [K]
- \( RH \): Relative humidity [%]
- \( V_p \): Vapor pressure [atm]
- \( AE \): Activation energy
- \( f \): Function of relative humidity [RH%]

A variation of approximately 0.5 to 1.0 eV has been reported in the activation energy corresponding to aluminum corrosion, which is due to several factors. Table 3-2 lists values for an estimated life based on actual environmental conditions (25°C, 55% RH, activation energy = 0.5 eV, and an acceleration rate that is proportionate to 4.5 times the humidity rate). The acceleration coefficient for testing under 85°C and 85% RH is a multiplier greater than 100. In other words, ten years of actual use can be simulated by implementing 1,000 hours of testing at 85°C and 85% RH.

The life estimate calculation expression is generally obtained from test results empirically, and the reason for the two calculation expressions shown in <3> above is that the constants employed in these two expressions differ depending on whether one assumes a correlation with the power of 2 of the relative humidity or a correlation with the inverse number of the relative humidity.

In calculating the acceleration rate, Arrhenius’ equation is used to calculate the acceleration coefficient of temperature, and the general powers equation is used to calculate the acceleration coefficient of humidity.
Therefore, the acceleration rate can be calculated as follows.

Temperature acceleration rate = \( \exp\left(\frac{(1/(T1-1/T2)) \times Ea/k}{\exp\left(\left(1/(25+273) \right) - \left(1/(85+273)\right)\right) \times 0.5/(8.6174 \times 10^{-5})}\right) \)
\[\cong 26.13\]

Humidity acceleration rate = \((RH2\%/RH1\%)\)^4.5
\[= (85/55)^4.5 \cong 7.10\]

Acceleration rate = Temperature acceleration rate \times Humidity acceleration rate
\[\cong 185.52\]

Table 3-2. Estimated Life under Actual Use Environment

<table>
<thead>
<tr>
<th>Temperature and Humidity Conditions for Moisture Resistance Test</th>
<th>Temperature and Humidity Conditions for Actual Use</th>
<th>Acceleration Coefficient</th>
<th>Test Period</th>
<th>Estimated Life</th>
</tr>
</thead>
<tbody>
<tr>
<td>85°C, 85% RH</td>
<td>30°C, 60% RH</td>
<td>91 times</td>
<td>1000 hours</td>
<td>10 years</td>
</tr>
<tr>
<td>25°C, 55% RH</td>
<td>186 times</td>
<td>1000 hours</td>
<td>21 years</td>
<td></td>
</tr>
</tbody>
</table>

(4) Countermeasures to improve moisture resistance

Moisture resistance can be improved in two ways.

\(<1>\) Passivation layer (protective layer) on chip surface

\(<2>\) Reduce moisture absorptivity and strengthen adhesiveness of resin

Concerning method \(<1>\), over 10 years ago semiconductor device manufacturers changed the material used for the passivation layer from SiO\(_2\) to SiN due to the latter’s superior adhesion strength and moisture resistance. However, while providing improved moisture resistance SiN layers also pose a problem due to the stress they apply on aluminum wiring and the silicon wafers. Currently, researchers are developing a new type of SiO\(_2\) layer that is less absorbent than ordinary plasma SiO\(_2\) layers.

Concerning method \(<2>\), Table 3-3 shows how introducing resins with low moisture absorptivity has improved useful life by an order of magnitude.

Table 3-3. Results of Moisture Resistance Tests on Resin with Low Moisture Absorptivity

| Resin | No. of Samples | Total Defects Detected, Preprocessing + PCT (Hours) |
|---|---|---|---|---|---|---|
| | | Preprocessing | 40 | 100 | 140 | 200 | 300 |
| Low-absorption resin | 20 | 0 | 0 | 0 | 0 | 0 | 0 |
| Standard resin | 20 | 0 | 1 | 3 | 6 | 9 | 14 |

Samples: 8-pin DIPs

Preprocessing: Temperature cycle

+ initial bake + 168 hours of moisture absorption testing at 85°C and 85% RH + solder dip at 260°C for 10 seconds,
+ repeat from initial bake

PCT test: 125°C, 2.3 atm
3.2.7 Cracks in passivation layer and aluminum slide

The recent trend toward on-chip implementation of an increasing number of functions has led to use of larger chip areas.

In addition, the wider use of surface mount devices has introduced greater environmental stresses such as thermal stress as chips become ever smaller and thinner.

Given this situation, various phenomena have been observed as leading to abnormalities such as cracking of the device-protecting passivation layer due to thermal stress on the resin (plastic) used in packaging and broken wires and/or shorting that occurs when aluminum wiring at chip corners is displaced.

Generally, the former phenomenon is called “passivation layer cracking” and the latter is called “aluminum wiring slide”.

[Mechanisms]
After a temperature cycle or thermal shock test is performed several times, thermal stress is produced by the differential thermal expansion between the silicon chip and resin. Specifically, the chip and the resin both expand when exposed to high temperatures. When they are subsequently placed in a low-temperature environment, the resin's contraction force causes the chip to contract toward its center, which places a shear strain on the aluminum wiring and the passivation layer on the chip's surface. When this strain exceeds the passivation layer's strength, cracks appear in this protective layer, viscosity-related deformation occurs in the aluminum wiring, and the aluminum wiring may slide away from its silicon substrate.

Figure 3-14. Diagram of Mechanisms (Temperature Cycle Testing, Low Temperature Phase)
[Countermeasures]
The following are general countermeasures for this problem.
(1) Reduce stress on resin materials
(2) Improve geometric shape of aluminum wiring
(3) Alleviate stress in resin with chip coating
(4) Redesign pattern layout at chip corners
3.2.8 Bonding wire-related failure modes

IC chips are electrically connected to external leads via thin wires made of gold or aluminum. Bonding wire-related failure modes include junction defects between the wire and chip, wire breakage, and wire-to-wire contact. Although most of these defects can be detected and sorted out as early defects by electrical inspections, in some cases the defects appear only after thermal stress or electrical stress has been applied.

Causes behind the above-mentioned failure modes include defective connections between bonding wires and pads, wire breakage at the wire’s neck area, and wire deformation.

(1) Formation of gold/aluminum alloy

There are two methods for bonding gold wire to aluminum pads: thermo compressive bonding and thermo compressive bonding combined with ultrasonic. Both methods use the mutual diffusion of gold and aluminum to make the bond. If mutual diffusion of gold and aluminum does not occur, the gold wire and aluminum pad do not bond, but the mutual diffusion can still be implemented by storing the device in an ambient temperature that exceeds the rated ambient temperature after bonding. However, in such cases, the different diffusion rates of gold and aluminum cause voids to occur near the junction, which can lead to wire breakage. Therefore, caution is required concerning the ambient temperature when subjecting such devices to thermal processing over a long period of time.

(2) Wire breakage at wire necks

When the wire necks are cut, some stress is applied to the base of the wire which lowers the wire’s strength and can lead to wire breakage. Photo 3-5 shows an example of this phenomenon. The causes of this stress include wire feed operations that are not smooth enough and mechanical vibrations that occur after the bonding wire process. Countermeasures in the manufacturing process include maintaining a smoother wire feed path and eliminating vibration during conveyance of devices between the bonding wire process and the encapsulation process.

Photo 3-5. Example of Damage at Ball Neck Area
(3) Wire deformation and wire-to-wire contact

During encapsulation using a mold resin, a resin tablet is inserted into a pot. Pressure from a plunger and heating of the metal die cause the resin to melt, after which it is injected into cavities via runners (see Figure 3-15).

The mold resin used in this case is thermosetting resin whose viscosity changes over time as heat is applied (see Figure 3-16). Although the best time to inject this resin into the cavities is when it is at its weakest viscosity level (see A to B in Figure 3-16), if something causes the resin to be injected when its viscosity level is high, enough stress may be applied to the bonding wire to cause wire deformation. Photo 3-6 shows an example of wire deformation as observed using X-ray equipment.

The deformation depends on the resin’s viscosity and fluid speed as it enters the cavities. Accordingly, extra caution is required when designing the metal die’s structure and when setting the resin molding conditions to avoid wire deformation.

![Figure 3-15. Molding in Die](image1)

![Figure 3-16. Characteristics of Thermosetting Resin](image2)

![Photo 3-6. Observation of Wire Deformation (Using X-Ray Equipment)](image3)
3.2.9 Thermal fatigue phenomena

(1) General
Thermal fatigue occurs when stress is applied during a thermal cycle to a structure in which materials having different thermal expansion coefficients are used for bonding. Due to the materials’ different thermal expansion coefficients, distortions are created repeatedly in the bonding area, which degrades the bonding strength and causes cracks in the bonding area. When thermal fatigue phenomena become more advanced, the bonding area may peel and cause wire breakage.

Some reliability problems have arisen concerning thermal fatigue in the solder that is used as a mounting material for heat-generating elements in semiconductor devices. When designing the materials to be used in heat-generating semiconductor devices, consider the materials’ physical characteristics, such as the thermal expansion coefficient and tests such as power cycle tests and temperature cycle tests should be performed to evaluate the effects of thermal fatigue on reliability.

(2) Failure modes and failure mechanisms
In the following example, which concerns a hybrid IC (hereafter abbreviated as “HIC”) that includes a power transistor (hereafter abbreviated as “PoTr”), failure modes and failure mechanisms related to thermal fatigue phenomena in mounting materials are described.

As a typical example of a failure mode related to thermal fatigue, let us consider the phenomenon of peeling of chip mounting materials in the solder layer. The failure mechanism is the process by which repeated ON/OFF operations by the heat-generating element’s PoTr chip creates a thermal cycle, during which deformation occurs in the solder mounting layers that are between materials having different thermal expansion coefficients, which causes the solder mounting layers to start peeling. Table 3-4 lists these failure modes and mechanisms. The structure of the PoTr section of the HIC used in this example includes four layers (from top to bottom): a PoTr chip layer, a metal layer, a substrate layer, and a heat sink layer. All of these layers are soldered together by solder mounting layers in which thermal fatigue is conspicuous. (See Figure 3-17.)

<table>
<thead>
<tr>
<th>Table 3-4. Failure Modes and Failure Mechanisms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure Mode</td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>Peeling of solder mounting layer</td>
</tr>
<tr>
<td>Cracking in solder mounting layer</td>
</tr>
<tr>
<td></td>
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<td></td>
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</tbody>
</table>

SOA: Safe Operating Area
(3) Improvement example

One improvement method for thermal fatigue at the solder mounting layer is to select (as the materials to be soldered) materials that have a thermal expansion coefficient that is roughly equivalent to that of the solder. Another method is to make the solder mounting layers as thick as possible. In the following example, the material used for the metal plate below the PoTr chip was changed to a material whose thermal expansion coefficient is roughly equivalent to that of the silicon, which effectively reduces degradation of thermal resistance due to thermal fatigue.

Power cycle tests were performed to compare and evaluate degradation of thermal resistance in the metal plate material before and after the material were changed. Before the material was changed, thermal resistance increased after about 3,000 cycles. After the material was changed, thermal resistance increased after about 10,000 cycles (see Figure 3-18).

An ultrasonic inspection device was used to compare and analyze thermal fatigue conditions on the solder mounting layers of a test sample of 4,000 cycles. Before the material was changed, peeling of the solder mounting layer due to thermal fatigue was observed but no such peeling was observed after the material was changed (see Figure 3-19).

These results indicate that changing the metal plate's material slows the progression of thermal fatigue phenomena and reduces degradation due to thermal fatigue.
Figure 3-18. Rate of Change in Thermal Resistance During Power Cycle Testing

\[ \Delta T_J = 125^\circ C \]
(15 minutes per cycle)

Rate of change in thermal resistance [%]

Before changing material

After changing material

No. of test cycles

Figure 3-19. Peeling of Solder Mounting Layer under PoTr Chip

Peeling occurs

Chip

Solder mounting layer (upper layer)

Metal plate

Power cycles: 2,000 to 3,000 cycles

(Note) Thermal expansion coefficient of metal plate is now closer to that of the chip.

No peeling was observed after changing metal plate material (Note)

Peeling (shown in red) was observed before changing metal plate material
3.2.10 Ion migration

(1) What is ion migration?
Also known as electrochemical migration, ion migration is the ionization of metal at the anode side when a voltage is applied between metal pins while moisture is present. Coulomb force causes the ionized metal to shift toward the cathode side. When the cathode side receives electrons, the ionized metal is deposited and grows as a metal.

Various metal materials are used in semiconductor device, including lead frame materials, plating materials, chip mounting materials, and bonding materials. Semiconductor devices are used in various fields such as automobiles, medical equipment and electronic equipment, caution is therefore required concerning how ion migration may occur under various use conditions and use environments. Ion migration in silver (Ag) is especially well known in semiconductor devices.

(2) Ion migration failure modes
Ion migration failure modes include withstand voltage degradation and dielectric degradation. Shorts between pins are rare; almost all failure modes involve an increase in leakage current (resistivity). When ion migration causes dendritic (branching) growth, heat generated when a current flows may cause breakage in some parts. Therefore, failures are occasionally recovered during testing or measurement.

(3) Mechanism for occurrence of ion migration
Three conditions must be satisfied for ion migration to occur: (1) an ionized substance, (2) moisture, and (3) an electric field. The following model has been proposed concerning the mechanism behind ion migration in silver (Ag).

<1> Ionization of Ag occurs at anode.
\[ \text{Ag} \rightarrow \text{Ag}^+ + e^- \]

<2> Ionized Ag\(^+\) reacts with ionized moisture.
\[ 2\text{H}_2\text{O} \rightarrow \text{H}_3\text{O}^+ + \text{OH}^- \]
\[ \text{Ag}^+ + \text{OH}^- \rightarrow \text{AgOH} \]

<3> Silver oxide is extracted from silver hydroxide, which is unstable.
\[ 2\text{AgOH} \rightarrow \text{Ag}_2\text{O} + \text{H}_2\text{O} \]

<4> The above reaction is reversible if moisture and an electric field are both present.
\[ 2\text{Ag}_2\text{O} + \text{H}_2\text{O} \rightarrow 2\text{AgOH} \rightarrow 2\text{Ag}^+ + 2\text{OH}^- \]

<5> Ag\(^+\) is shifted toward the cathode by coulomb force, and where it is extracted as Ag.
\[ \text{Ag}^+ + e^- \rightarrow \text{Ag} \]
(4) Acceleration conditions for ion migration

Ion migration occurs in silver whenever the required moisture and voltage conditions exist. However, ion migration accelerates depending on the following four other conditions: <1> temperature, <2> humidity, <3> electric field strength, and <4> contamination by ionic impurities such as halogen or alkali.

Without taking contamination by ionic impurities into consideration, Ag migration that occurs between two electrodes in the dielectric substrate can be expressed by the following formula.

\[ t = A \cdot E^{-r} \cdot H^{-n} \cdot \exp \left( -\frac{E_a}{kT} \right) \]

where:
- \( t \): Time when migration occurs
- \( E_a \): Activation energy
- \( A \): Acceleration constant determined according to dielectric substrate material
- \( k \): Boltzmann's constant
- \( E \): Electric field strength
- \( r \): Constant
- \( H \): Humidity
- \( n \): Constant
- \( T \): Absolute temperature

(5) Silver migration in semiconductor devices

Although silver migration seldom occurs in semiconductor devices, it can occur when all three of the following conditions exist: (1) too much Ag paste was applied when mounting the chip to the lead frame, (2) a positive potential is applied to a chip surface that had poor adhesion with the adjacent resin, and (3) temperature/humidity conditions encourage silver migration.

The external pins in a semiconductor device are sometimes exposed to the ambient air. In such cases, in addition to caution regarding Ag migration, caution is required with regard to silver sulfide whiskering that can occur even under unbiased conditions when the ambient air contains hydrogen sulfide.

3.2.11 Degradation of optical characteristics in LEDs (Light Emitting Diodes)

(1) Dark line defects in LEDs

To better understand the degradation of optical characteristics in laser diodes, let us first briefly examine how optical characteristics are degraded in LEDs.

When LEDs are operated under a relatively high current density, lines that do not emit light appear in the light-emitting region. These lines are called "dark lines." These dark lines are a series of dislocations within the crystal's active layer, which can occur when the LED is being operated.

There are actually two types of dislocations: One that always occurs due to the <100> crystal orientation and that is the principal cause of <100> dark lines, and another that is due to dark line growth that occurs with the <110> crystal orientation.

In InGaAsP LEDs that operate with a 1 µm wavelength, dark lines in the <100> direction are less likely to occur. This is due to the crystal material, which offers excellent resistance to dark line defects. However, dark lines in the <110> direction are likely to occur when crystal lattice defects cause misfit dislocation, when defects occur during stripe formation, or when strong distortion occurs in ohmic electrodes.
(2) Prevention of dark line defects in LEDs

First, to address the growth of dark lines due to dislocations that occur due to the <100> crystal orientation in the active layer, use dislocation-free substrates, improve the quality of crystals, or encourage epitaxial growth in a clean environment. To avoid dislocation during operation that is triggered by distortion present in the <110> crystal orientation, reduce crystal distortion. More specifically, use heat sink materials whose thermal expansion coefficient approximates that of crystal. Therefore, a silicon-type material whose thermal expansion coefficient approximates that of crystal is used for LED heat sinks, and an alumina-type material is used for long wavelength devices.

(3) Dark line defects in laser diodes

In laser diodes, degradation causes the threshold current density to rise while lowering external differential quantum efficiency.

Because of these phenomena, the I-L characteristics of the CW operation change from (1) through (5) as shown in Figure 3-20, and finally CW operation becomes impossible.

![Figure 3-20. Changes over Time in I-L Static Characteristic](image_url)

Degradation phenomena found in laser diodes are caused by damaged mirror facet or changes in the condition of other surfaces. Most of the causes are the same as causes leading to degradation of LEDs. This degradation accelerates at higher temperatures, or with higher optical output and higher operating current density.

There are two types of dislocation-based degradation mechanisms. One is due to the “dislocation web” (dark lines that occur as dislocation increases after repeated discharge and absorption of point defects). These dark lines are the same as the <100> dark lines that are found in LEDs.
Dislocation penetrating the active layer or nonradiative recombination caused by point defects discharges energy, which, through lattice vibration, generates and moves the point defects. This is thought to contribute to the upward and downward movement of dislocation.

As a result, the dislocation becomes twisted in some parts of the active layer, and this deformation creates dislocation "arms" whereby dark lines appear as this dislocation expands in the active layer. When crystal defects are caused by this type of nonradiative recombination in an injected carrier, point defects result in dislocation (a phenomenon generally known as recombinant defect migration).

When these dark lines are observed on the surface (001), they are oriented in the <100> direction. This is because dislocation that occurs in a thin active layer always grows from surface (100) toward the angled surface (110). Such growth does not occur on clad layers that do not undergo excitation, but rather spreads within active layers.

The occurrence of dark lines increases absorption loss of nonradiative recombination and in laser resonators, eventually increasing CW threshold current.

The increase in the threshold current influences the laser diode's operation conditions, leading to failures in applications. The higher the temperature and the current density are, the higher the growth of dark lines accelerates.

Types of dislocation that generate dark lines include (1) "through dislocation" whereby dislocation that occurs in the substrate crystal spreads to the surface of the epitaxial layer; (2) dislocation that occurs due to hetero junctions; (3) and dislocation that occurs due to precipitate. In InGaAsP lasers, there is also "misfit dislocation" that is due to irregular lattice formation.

The other type of dislocation is dislocation caused by stress applied during operations. In other words, dislocation starts in regions where the crystal surface is weak, then spreads to the active layer where it continues to grow. In such cases, all of the points are slippage of dislocation, which create dark lines in the <110> direction.

(4) Prevention of dark line defects in laser diodes

To suppress the aforementioned types of dislocation as much as possible, the following measures are generally adopted: (1) use of substrates with low dislocation density, (2) epitaxial growth in a clean environment, (3) addition of elements with strong gettering effect (e.g. Al and Mg) to the liquid solution, (4) reduction of the concentration of easily extracted impurities, and (5) regular lattice formation.

Accordingly, several elements that contribute to dark line-related degradation can be eliminated by implementing these types of improvements and by checking for changes in threshold current values before and after burn-in testing. In addition, stress-induced dislocation can be prevented by using heat sinks whose thermal expansion coefficient approximates that of the laser diode.

References

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• “Reliability Engineering for Semiconductor Devices,” Matsushita Electric Industrial Co., Ltd. editor, JUSE, pp.156 to 163 (Japanese version only)
• Nikawa, K., S. Yama and T. Yoshida, “Fault analysis of devices and parts,” JUSE, pp.88, 89 (Japanese version only)
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3.3 Faults in Use Environment

3.3.1 Electrostatic discharge (ESD)

Electrostatic discharge (ESD) has become a serious issue as a result of the ongoing ultra-fine processing and high integration of semiconductor devices. Models for the occurrence of ESD and the related failure modes are described below.

(1) Models for ESD occurrence

The occurrence of ESD causes degradation of certain semiconductor device characteristics (such as increased leakage current, degradation of withstand voltage, variation of $h_{FE}$, and short or open state). Three models have been proposed to describe the causes of the ESD that causes such degradation.

- **<1> Human Body Model (HBM)**
  This model describes damage that occurs when static electricity is discharged to a device that is touched by an electrically charged human body.

- **<2> Machine Model (MM)**
  This model describes damage that occurs when static electricity is discharged to a device that is touched by a manufacturing equipment unit that can carry a much larger electrical charge than the human body.

- **<3> Charged Device Model (CDM)**
  This model describes damage that occurs when static electricity, such as that built up by friction between device packages or lead frames, is discharged via a device’s pins.

Testing methods that reproduce these models are based on the standards listed in Table 3-5. Both sets of standards are premised upon the human body model and the machine model.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Condition</th>
<th>Times Applied</th>
</tr>
</thead>
</table>
| MIL-STD-883C Method 3015 | 100 pF 1.5 kΩ | Class 1: 0 V to 1999 V  
                          |                   | Class 2: 2000 V to 3999 V  
                          |                   | Class 3: 4000 V and above  | 3 times |
| EIAJ ED-4701           | 100 pF 1.5 kΩ | 1000 V        | 3 times |
| EIAJ ED-4701 (Reference test) | 200 pF 0 Ω | 150 V         | 1 time  |
(2) Charged device model (CDM)
Among the various recent ESD models, the most threatening model for semiconductor devices has been the CDM characterized by high-speed discharges. The CDM includes three mechanisms for the discharge of electrical loads.

<1> Phenomenon: induced electrification phenomenon due to electric field generated by electrostatic load near IC chip
Static electricity is generated when friction occurs on the surface of an IC package. A similar phenomenon occurs near charged CRTs or insulators. The electric field that creates the electrostatic charge is also the inductor for the dynamic charge that is drawn to the IC’s internal conductor.

<2> Phenomenon: when an IC’s lead touches a charged conductor, the electrostatic capacity $C_{LG}$ between the IC’s internal conductor and GND is charged.
As a typical example, consider the phenomenon that occurs when a charged human body touches an IC’s lead. However, generally speaking, the IC is not damaged during such discharges because the conductor’s resistance increases the time constant for discharge.

<3> Phenomenon: ESD that is discharged from the surface of a charged insulator to an IC lead
In this case, the IC can be damaged as soon as the discharge occurs. Even if it is not damaged then, it is still charged and will be damaged later by the CDM mechanism.

The dynamic load related to the above phenomena flows very quickly if the IC lead is grounded, which damages the IC. In a charged IC that is not electrically neutral, this dynamic load is regarded as an excess load. Therefore, the dynamic load related to the above three phenomena is defined as an excess dynamic load.

Breakdown resistance and CDM management methods on production lines are described later.

(3) Testing methods
Figure 3-21 shows a basic circuit configuration of CDM test equipment. First, the load $Q$ that is charged by voltage $V$ in the IC’s internal conductor is measured (the structure of the load meter is described later). At that point, the electrostatic capacity $C_{LG}$ between the IC’s internal conductor and GND can be calculated as $C_{LG} = Q/V$ (the applied voltage $V$ is already known). Next, the IC is again charged at the same voltage and is connected to a ground. Finally, an IC tester is used to check for degradation in the IC.

In sum, after a probe touches one pin, switch shifting moves from left to right. In other words, the test sequence starts with charging, then proceeds to measuring the charge, recharging, and grounding.

Figure 3-21. CDM Test Equipment
(4) Test results

As shown in Figure 3-22, the breakdown voltage for MOS ICs is inversely proportional to the electrostatic capacity. This means that breakdowns occur at a constant load value $Q_0$. Although breakdown traces could not be confirmed even when using a scanning electron microscope with approximately 20,000× magnification, after testing it was found that all samples had electrically shorted at MOS FET gates downstream from protection circuits.

Figure 3-22. CDM Test Results of MOS ICs
(5) Breakdown modes

<1> Junction breakdown (see Photo 3-7)

A junction breakdown is a thermal breakdown phenomenon that occurs when an excess load flows in the reverse bias direction relative to a PN junction. The failure is located either at the junction of the shortest sections where the load flows or at a location where a junction is curved. There are also cases in which the damage cannot be determined, such as when there is an increase in leakage current or degradation of withstand voltage.

Photo 3-7. Examples of Junction Breakdown

<<Microscope photo after etching>>

3600x

CDM application pin → pin 364

Trace of breakdown cannot be confirmed

<<SEM photo after etching>>

@: Location of breakdown is confirmed
Oxide layer breakdown (see Photo 3-8)
The silicon oxide layer's dielectric breakdown strength is approximately 10 MV/cm. In MOS type semiconductor devices, there is a very thin gate oxide layer that enables dielectric breakdowns to occur in the oxide layer at relatively low voltage. For example, if the gate oxide layer's thickness is 300 Å, a dielectric breakdown may occur when the voltage is about 30 V. In actual products, there are gate oxide layer protection circuits comprised of resistors and diodes that boost resistance to such breakdowns. Nevertheless, MOS-type semiconductor devices must be handled with extra care since they are prone to dielectric breakdowns.

Photo 3-8. Example of Oxide Layer Breakdown
(6) CDM management methods in manufacturing lines

A basic equivalent circuit for a load meter is shown in Figure 3-23. The excess dynamic load \( Q_{EM} \) that is charged to the IC’s electrostatic capacity \( C_{EM} \) comes into contact with an existing capacitor \( C \) whose capacity is roughly two orders of magnitude greater than the electrostatic capacity \( (C_{EM}) \) at the IC’s lead. If the capacitor’s pin voltage is subsequently measured, the excess dynamic load \( Q_{EM} \) can be determined (as \( Q_{EM} = C \times V \)).

This load meter can be used to directly measure the constant breakdown charge capacity \( Q_{EM} \) [C] in a MOS IC, which is the breakdown factor in the CDM for ICs. The electrostatic capacity \( C_{LG} \) of the IC’s internal conductor and the charge voltage \( V \) can be used to express the breakdown resistance capacity used in CDM testing of MOS ICs as a constant charge capacity \( Q_D = V \times C_{LG} \) [C].

However, manufacturers of IC products and electronic equipment measure only the “potential” of a charged body and have established their empirical control standards for the maximum allowable potential. Consequently, there are various divergent measurement results and failure prevention measures. Still, it remains possible to resolve this issue by using a load meter.

The suitability of countermeasures can be judged by measuring the excess dynamic load \( Q_{EM} \) of ICs taken from random locations on the production line floor and comparing these measurements with the resistance values and measured energy and load values obtained from IC breakdown tests.

Figure 3-23. Electric Charge Meter
3.3.2 Latchup

(1) General
Due to unrivaled features such as low power consumption, CMOS ICs have become the most popular type of IC on the market today. However, CMOS ICs are also unique in terms of breakdown in that they are the only type to experience latchups, which have posed problems in some cases.
This section describes latchup phenomena and then explains latchup testing to measure latchup resistance in CMOS ICs. It also lists cautions on preventing latchup.

(2) Mechanism of latchups
The CMOS structure includes a PNPN thyristor-type structure comprised of parasitic transistors between the V_{DD} and V_{SS} power supply pins. Latchup occurs when a parasitic thyristor is activated by noise or other events from an external source, which basically causes a short between V_{DD} and V_{SS} and thereby allows a large current to flow continuously until the power is shut off, which in turn can cause overcurrent-related damage.
The latchup mechanism is explained below with reference to an inverter that is presented as a typical CMOS circuit. A circuit diagram of the CMOS inverter is shown in Figure 3-24, its structure is shown in Figure 3-25, and an equivalent circuit that includes parasitic transistors is shown in Figure 3-26 to describe latchup phenomena.

![Circuit Diagram of CMOS Inverter](image)
As shown by the path indicated as a broken line in Figure 3-25, this circuit contains a parasitic thyristor. Since latchup sets an ON state in the parasitic thyristor, the base for Tr2 or Tr6 is triggered by an event such as external noise. Latchup may occur when the base of Tr2 or Tr6 is triggered. The latchup triggering mechanism for when Tr6 is ON is described below.
<1> When an external noise, surge, etc., is applied to the circuit, current flows temporarily to R2 and the voltage drop on both ends is greater than the voltage required to set Tr6 to ON.

↓

<2> Tr6 is set to ON and current flows to R1.

↓

<3> Voltage drop at both ends of R1 is greater than the voltage required to set Tr2 to ON.

↓

<4> Tr2 is set to ON and current flows to R2.

↓

<5> If the voltage drop on both ends of R2 is held at or above the voltage level required to set Tr6 to ON, current flow is maintained between VDD and VSS and latchup occurs.

Even at stage <4> above, where a rather large current is flowing, if the voltage on both ends of R2 is within the ON voltage level for the parasitic thyristor, latchup does not occur because the parasitic thyristor is not set to ON. The large-current flow occurs for only an instant before the current value returns to the previous level. If the hFE product for Tr2 and Tr6 is “1” or greater, the parasitic transistor’s ON status is held and latchup occurs. In ordinary CMOS ICs, this product is “1” or greater, and therefore latchup can occur. The same is true when Tr2 is triggered first.

The following causes of latchup can be considered when Tr2 or Tr6 is triggered.

<1> When voltage at I/O pins is greater than VDD or less than VSS

\[ \text{Vin} > \text{VDD} \]
\[ \text{Vin} < \text{VSS} \]
\[ \text{Vout} > \text{VDD} \]
\[ \text{Vout} < \text{VSS} \]

<2> When power supply voltage VDD rises

<3> When power supply voltage VDD changes suddenly (sudden rise)

A situation in which Vin > VDD is considered as an example of the latchup mechanism for condition <1> above.

\[ \text{Vin} > \text{VDD} \]

↓

Current flow: \[ \text{Vin} \rightarrow \text{R3} \rightarrow \text{Tr1 between E and B} \rightarrow \text{R1} \rightarrow \text{VDD} \]

↓

Tr1 is set to ON, current flow: \[ \text{Vin} \rightarrow \text{R3} \rightarrow \text{Tr1 between E and C} \rightarrow \text{R2} \rightarrow \text{VSS} \]

↓

Tr6 is set to ON and latchup occurs.

Under other conditions, the principle is almost the same: Tr2 or Tr6 is set to ON and latchup occurs. Actually, noise occurs across the I/O pins, and latchup can occur when the voltage is greater than the power supply voltage or less than the GND potential (VSS).

Under condition <2>, latchup is caused when a breakdown occurs between E and C for Tr2 or Tr6. This can occur when noise enters the power supply line.

Under condition <3>, latchup is caused when the power supply voltage suddenly changes, causing a discharge current to flow across the junction capacitance between the substrate and well, which triggers the parasitic thyristor and generates latchup. In practice, this tends to occur the moment the device’s power is turned on.
Usually, a destructive mode due to latchup is classified as an overcurrent destructive mode since an overcurrent flow from VDD to VSS causes burnout of Al wires of VDD or VSS and melting of bonding wires. Even when latchup is caused by noise across the I/O pins, in most cases the damage is located on the wiring to either VDD or VSS, and it is usually impossible to identify which pins the noise will traverse. This makes it difficult to pinpoint causes and implement effective countermeasures.

(3) Latchup resistance measurement methods

There are three methods for measuring latchup resistance.

<1> Pulse current injection method

The stable-current pulse injection method consists in gradually applying a stable trigger pulse current to the target device's I/O pins while a power supply is being applied and checking the device for latchup. Latchup is detected by a change in the power supply current value. The pulse current value when the power supply current exceeds the rated value is taken as the measurement of the target device's latchup resistance. Figure 3-27 shows a test circuit diagram for the pulse current injection method.

<2> Power supply overvoltage method

The power supply overvoltage method consists in superposing a trigger pulse voltage on the power supply voltage and checking the device for latchup. Latchup is detected by a change in the power supply current value. The pulse current value at the time when the power supply current exceeded the rated value is taken as the measurement of the target device's latchup resistance. Figure 3-28 shows a test circuit diagram for the power supply overvoltage method.
Figure 3-28. Power Supply Overvoltage Method

Input pins are connected to power supply (Vcc) or GND pin
Output pins are left open

Figure 3-29. Capacitor Voltage Application Method

Variable power supply (dual polarity)

(4) Prevention of latchup
The following measures can be implemented during IC design to prevent latchup phenomena.
<1> Prevent variation in potential by setting frequent contacts with substrate or well.
<2> Use epitaxial wafers to lower wafer resistance and to prevent voltage increases when a current is flowing.
<3> Use a thick oxide layer and a guard ring to separate elements.
<4> Use a thick oxide layer and a channel stopper to separate elements.

Capacitor voltage application method (for reference)
The capacitor voltage application method consists in gradually charging a capacitor at a certain voltage, then applying the capacitor's discharge voltage to the target device and checking the device for latchup. Figure 3-29 shows a test circuit diagram for the capacitor voltage application method.
3.3.3 Breakdowns in power MOS FETs

Since power MOS FETs are voltage-driven devices, they enable direct control at high power ratings via ICs such as CMOS ICs. Compared to bipolar power transistors, power MOS FETs offer faster switching, lower dissipation, and larger safe operating areas. Thus, power MOS FETs are finding greater use in response to market needs centered on high-speed switching applications.

Recently, various breakdown problems have arisen as demand rises for power MOS FETs that combine higher performance with smaller size. This section describes the structure of power MOS FETs, safe operating areas and breakdown modes, and overvoltage-related damage in the gate oxide layer.

(1) About power MOS FETs

Power MOS FETs have the same basic structure as ordinary MOS FETs. However, various extra design elements, such as a high-withstand voltage structure and low on-resistance, have been added to provide the features required in power MOS FETs. The two main distinctive features of power MOS FETs are described below.

<1> In N-channel MOS FETs, the source region has a double-diffused MOS FET structure featuring a low-concentration p layer that includes a high-concentration n layer.

<2> A large number of FET cells are arranged in parallel to increase the channel width and lower the on-resistance.

The structure of a typical power MOS FET and an equivalent circuit are shown in Figure 3-30.

Figure 3-30. Power MOS FET Structure and Equivalent Circuit
(2) Safe operating areas and breakdown modes in power MOS FETs

The safe operating area of a power MOS FET is divided into two types: forward bias safe operating area (hereafter called “forward SOA”) and reverse bias safe operating area (hereafter “reverse SOA”). The forward SOA is the safe operating area where the gate and source voltage is forward-biased. As shown in Figure 3-31, this area’s boundaries consist of four lines: the on-resistance limit line (A), pulse drain current limit line (B), power dissipation line (C), and drain-source withstand voltage line (D). Operations within the forward SOA are usually free of breakdowns or other abnormalities. However, various abnormalities will occur if operations use an area beyond the forward SOA. Figure 3-31 shows the relation between the forward SOA and various failure modes.

Figure 3-31. Forward SOA and Failure Modes (Failure Modes Are Encircled)

<1> Bonding wire break
When an excessive current flows on a bonding wire, the wire may heat up and fuse. Therefore, caution is required to avoid exceeding the rated current value per unit area of wire.

<2> Failure due to thermal runaway
Since power MOS FETs are majority-carrier devices, unlike bipolar transistors they are not prone to secondary breakdowns in high-voltage areas. The thermal runaway phenomenon is also less likely to occur than in bipolar devices, due to the larger SOA. However, an excess power situation may still occur when a high voltage and large current is applied. There is a chance that thermal runaway may occur when the junction temperature becomes extremely high. When the ambient temperature is high, the device’s guaranteed temperature may be exceeded at power settings that would be safe when the ambient temperature is low. Therefore, be sure to derate the operating conditions for actual use.

<3> Overvoltage failure
When an excessive voltage is applied to a power MOS FET’s drain-source withstand voltage, a parasitic diode between the source and drain breaks down, causing a failure.
(3) Overvoltage breakdown of gate oxide layer

To realize low dissipation, the power MOS FET’s gate electrode is insulated by a thin oxide layer. The electric field strength on the gate oxide layer is designed to remain below the oxide layer’s breakdown voltage (intrinsic breakdown voltage: approximately 10 kV/cm), so there is no problem as long as the voltage applied to the gate pin is within the rated value. However, if an overvoltage (due to static electricity, etc.) is applied to the gate electrode, an electric field that exceeds the intrinsic breakdown voltage is applied to the oxide layer and may cause a breakdown.

One countermeasure for such breakdowns is clamping to prevent a voltage that is greater than the intrinsic breakdown voltage from being applied to the gate oxide layer. An example of this type of countermeasure is shown in Figure 3-32. In this countermeasure, polycrystalline silicon is used on the oxide layer and a Zener diode and a gate protective resistor are added in series between the gate and source to prevent application of an overvoltage to the gate electrode.

Figure 3-33 shows an improved version with higher electrostatic discharge (ESD) breakdown resistance.

Figure 3-32. Gate Electrode Protection Circuit
Figure 3-33. Effect of ESD Breakdown Resistance Improvement Using Protective Diode and Protective Resistor

![Diagram of ESD test circuit](image)

ESD test circuit
(Apply + or − between gate and source. Apply once.)

<table>
<thead>
<tr>
<th>Percentage remaining (%)</th>
<th>Applied voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td>0</td>
<td>300</td>
</tr>
<tr>
<td>Without protective diode for gate</td>
<td>400</td>
</tr>
<tr>
<td>With protective diode for gate</td>
<td>500</td>
</tr>
<tr>
<td>With protective diode for gate + protective resistor for gate</td>
<td>600</td>
</tr>
</tbody>
</table>

References
- IEEJ editor, "Power Device and Power IC Handbook" Corona Publishing Co., Ltd. (Japanese version only)
- "Development of Industrial Power MOS FET DIII and DIV Series" Hitachi Review, 72, 12, p87 (1990) (Japanese version only)
### Package cracking during mounting

Although in small quantity, a plastic package absorbs moisture even when it is stored at room temperature. If the surface mounted type package absorbing moisture is subjected to thermal stress due to soldering, the following problems may arise:

- **<1>** The package surface may be expanded or cracked (see Photo 3-9.)
- **<2>** The reliability of the IC may be degraded.
- **<3>** The chip may be damaged due to aluminum slide, etc.
- **<4>** The bonding wire may break.

This section describes the mechanism and causes of these problems, their countermeasures, and the moisture absorption and dry characteristics of plastic packages.

#### (1) Mechanism of package crack

Figure 3-34 illustrates how a package crack occurs. The following paragraphs describe the outline of each cause of crack occurrence:

**Figure 3-34. Mechanism of Package Crack Occurrence**

1. **Moisture**
   - **(i) Moisture absorption of package**
     - Bulk absorption
     - Surface absorption
   - **(ii) Mounting process**
     - Abrupt thermal stress
     - Abrupt rise of package temperature
   - **(iii) Increase in internal force of package**
     - Vaporization and expansion of absorbed moisture
     - Difference in thermal expansion of each material
   - **(iv) Occurrence of surface peeling**
     - Concentration of internal force
     - Peeling occurrence mode ratio
       - (a) > (b)
   - **(v) Occurrence of package crack**
     - Decrease in internal force
     - Crack occurrence mode ratio
       - (A) > (B) > (C)
(a) Moisture absorption of package

The plastic package is made of epoxy-based mold resin. When stored at room temperature, this epoxy resin absorbs a small amount of moisture contained in the air.

Figure 3-35 and 3-36 show examples of the moisture absorption behavior of packages.

Photo 3-9. Cross-Sectional View of Package Crack

These figures indicate that a thin type SMD absorbs moisture up to 0.36 wt% when it is stored outdoors, and up to 0.27 wt% when stored indoors (in Tokyo).

The maximum moisture absorption when the sample is stored outdoors is equivalent to a saturated absorption rate at about 30°C, 75% RH, and that when the sample is stored indoors is equivalent to a saturated absorption rate at about 25°C, 65% RH.

The maximum value was observed in summer when the temperature and humidity rise, and the minimum value was recorded in winter when the temperature drops.

Based on these data, Compound Semiconductor Devices Division specifies, as moisture processing conditions, 30°C, 85% RH for the products for which moisture control is not necessary, and 30°C, 70% RH for the products for which moisture control is necessary (both conditions are determined by taking into consideration areas where temperature and humidity are high).

(b) Mounting process (thermal stress application)

When a package that has absorbed moisture is mounted on a PWB and is then subjected to an abrupt thermal stress (especially if the package is mounted by means of a general heating method), the package temperature rises abruptly.

(c) Increase in internal force of package

When the temperature rises, the moisture absorbed by the package is vaporized and expanded, generating a great stress inside the package. In addition, because the package is heated, the strength of the resin is degraded and differences in the thermal expansion rate of each constituent elements occur. (Figure 3-37 shows changes in the characteristics of the resin due to temperature rise. This figure indicates that the thermal expansion coefficient of the resin substantially increases, and the bending strength substantially drops if the temperature exceeding the glass transfer temperature.)

(d) Occurrence of surface peeling → concentration of internal force

Surface peeling occurs if the stress generated inside the package exceeds the adhesive force of the resin and inserted parts (lead frames and IC chip). This phenomenon most likely occurs on the rear surface of the island that does not so tightly adhere to the resin but occupies the largest area in the package. As a result of peeling, the package may expand and stress is concentrated on the edge part of the peeling.
(e) Occurrence of package crack

The package is cracked if the stress concentrated on the edge of surface peeling exceeds the strength of the resin. If the internal stress generated is too great, or if adhesion between the resin and chip surface is not enough, peeling may also occur on the surface of the chip, or the package may be cracked. This phenomenon may lead to damage to the chip surface or a break of the bonding wires. Peeling of this type causes direct penetration of water or impurities onto the chip surface or corrosion of aluminum wiring (leading to degradation of the moisture resistance of the device).

Figure 3-35. Moisture Absorption Behavior of Package Stored Outdoors for One Year

![Figure 3-35](image1)

Figure 3-36. Moisture Absorption Behavior of Package Stored Indoors for One Year

![Figure 3-36](image2)
Figure 3-37. Dependency of Bending Strength and Thermal Expansion Coefficient of Insulated Resin on Temperature
(2) Causes and influences of package crack

The following factors are the principal causes of package cracking (or degradation of moisture resistance):

<Factors>
<1> Moisture absorption of package before soldering and mounting
<2> Mounting conditions
<3> Package structure
  • Island size
  • Package thickness

(a) Moisture absorption of package before soldering and mounting

Figure 3-38 shows the influences of the moisture absorption of the package on the SMD before the device is soldered and mounted.

This figure illustrates the relations between the threshold moisture absorption rate and time when thermal stress of infrared reflow soldering is imposed on the sample.

The threshold moisture absorption rate, beyond which the package is cracked, is 0.18 wt% when the sample is stored at 85°C, 85% RH for 14 hours, and 0.125 wt% when the sample is stored at 30°C, 70% RH for 192 hours.

Figure 3-39 shows a moisture concentration model in the package when a crack occurs. The moisture concentrations on the rear surface of the island (metal plate on which the chip is placed) coincide when the crack has occurred. Therefore, it can be concluded that the package crack is dependent upon the moisture concentration on the rear surface of the island, not upon the moisture absorption rate.
(b) Influence of mounting conditions on device reliability (moisture absorption and cracking)

Figures 3-40 and 3-41 show the effects of soldering conditions (soldering method, temperature, and time) on device reliability (resistance to moisture and cracking). These results show that the reliability of a device (in terms of resisting moisture absorption and cracking) depends greatly on the soldering method and the heating conditions for soldering.

Figure 3-40. Effects of Soldering Conditions on Moisture Resistance
Figure 3-41. Relation Between Package’s Internal Temperature and Package Cracking

- Infrared reflow (220°C)
- Infrared reflow (240°C)
- Infrared reflow (260°C)
- Hot air reflow (240°C)
- Infrared + hot air reflow (240°C)
- VPS (215°C)
- Wave soldering (260°C)

Sample: Plastic PKG product (80-pin QFP, 2.7 mm thick)

Thermocouple

Measurement point for internal temperature

Island rear surface moisture level when package cracking occurs (mg/cm³)

Package’s internal temperature (island rear surface) [°C]
(c) Package structure

Figures 3-42 and 3-43 show simulation results concerning the relation between island size and moisture concentration on the island’s rear surface during package cracking. These results show that package cracking is more likely to occur as the island size becomes larger. Figure 3-42 shows that cracking is less likely to occur as the package becomes thicker. Figure 3-43 shows that cracking can be suppressed even for large islands by lowering the reflow temperature.

Figure 3-42. Relation Between Package Thickness and Moisture Concentration

Figure 3-43. Relation Between Peak Reflow Temperature and Moisture Concentration
(3) Preventive measures

Given the causes of package cracking described above, Figure 3-44 shows a model of how each cause relates to the entire phenomenon. The following points are drawn from this model as measures to prevent package cracking and degradation of moisture resistance as well as to enlarge the safety area.

<Points>
<1> Devise control measures to minimize the package's moisture absorption rate.
<2> Select a soldering method that features low thermal stress.
<3> When soldering, keep the soldering temperature as low as possible.
<4> Whenever possible, select a thick package.

Figure 3-44. Model of Factors Behind Package Cracking
(4) Moisture absorption and drying

(a) Moisture absorption characteristics at 25°C, 65%

Figure 3-45 shows the moisture absorption characteristics of QFPs of various epoxy resin thickness when the packages are stored at an ambient temperature (Ta) of 25°C and a relative humidity (RH) of 65%. The vertical axis of this figure indicates the moisture absorbed by the packages divided by the resin weight at the beginning of storage and expressed in percentage. The horizontal axis indicates the lapse of time. As shown in this figure, the moisture absorption rate varies depending on the thickness of the resin, i.e., the thinner the package, the quicker the package absorbs moisture.

It is recommended that Compound Semiconductor Devices Division’s packages be stored at 25°C, 65% RH after the dry pack is opened.

Figure 3-45. Moisture Absorption Characteristics (25°C, 65% RH)
(b) Moisture absorption characteristics at 30°C, 70% RH

Figure 3-46 shows the result of moisture absorption characteristic simulation (calculated value) at 30°C, 70% RH. Compound Semiconductor Devices Division conducts its humidification processing test at 30°C, 70% RH on the products for which moisture absorption must be controlled. This condition complies with the JEITA (Japan Electronic Industry Development Association) standard (30°C, 70% RH: moisture absorption control necessary).

Figure 3-46. Moisture Absorption Characteristics at 30°C and 70% RH (Calculated Values)
(c) Moisture absorption characteristics at 30°C, 85% RH

Figure 3-47 shows the result of moisture absorption characteristic simulation (calculated value) at 30°C, 85% RH. Compound Semiconductor Devices Division conducts its humidification processing test at 30°C, 85% RH on the products for which moisture absorption control is not necessary. This condition complies with the JEITA standard (30°C, 85% RH: moisture absorption control is unnecessary). Because it takes a long time to test under conditions of 30°C, 85% RH, the test time is shortened by actually conducting an equivalent test at 85°C, 85% RH so that the same amount of moisture is absorbed.

Figure 3-47. Moisture Absorption Characteristics at 30°C and 85% RH (Calculated Values)
(d) Drying temperature characteristics

Figure 3-48 shows the moisture absorption of a sample equivalent to when the sample is baked at 125°C for 10 and 20 hours, respectively, when the sample is baked at the lower temperatures. This data is shown for your reference if you need to bake at the lower temperatures. As shown, the baking time at 90°C is about seven times that at 125°C. If the sample is baked at 70°C, the baking time is about 15 times longer than at 125°C.

Note that if the sample is baked at 70°C, and when the moisture absorption rate has dropped below 0.1 wt%, the sample cannot be dried further depending on the environment. Also note that too long a baking time may cause oxidization of the leads.

Figure 3-48. Drying Characteristics

References
- EIAJ-ED-4701-2 "Environmental and Endurance Test Methods for Semiconductor Devices"
- NEC Electronics "Semiconductor Device Mount Manual"
3.3.5 Secondary breakdowns in power transistors

A failure that involves momentary and unrecoverable shorting between the collector and emitter can occur during a power transistor’s switching operations even when the operating conditions are within the rated voltage, rated current, and allowable dissipation. This phenomenon is called a secondary breakdown.

Figure 3-49 shows safe operating areas (SOAs).

Secondary breakdowns include forward secondary breakdown that is observed when the transistor is operated in active area (base is forward biased) and reverse secondary breakdown that is observed when the transistor is turned off.

In the data book, the breakdown resistance values for these types of breakdowns are guaranteed based on a forward bias SOA curve and a reverse bias SOA curve.
As shown in Figure 3-50, when a switching operation is performed for an inductive load in an ordinary transistor, there are operation traces from [A] to [B] during turn-on, and from [B] to [A], during the turn-off, in the cut-off area [A] and the saturated area [B].

The relative safety of switching operations can be determined by confirming whether the operation traces of the turn-on and turn-off operations are within the areas rated as the forward bias SOA and reverse bias SOA, respectively.

[Failure mode in forward secondary breakdown]
The base current flows from the base electrode to the emitter. At that point, current is concentrated at the periphery of the emitter and a fringing effect occurs. When current concentration occurs, the local temperature starts to rise. As the temperature rises, a positive feedback effect lowers the resistance at the warming areas, which allows more current to enter until the silicon itself melts, resulting in "hot spot" damage. As an improvement to reduce such current concentration, some devices have a structure that also includes ballast resistors in the emitter stripe.

[Failure mode in reverse secondary breakdown]
Reverse secondary breakdowns occur when the transistor is performing high-speed operations under an inductive load. During the turn-off state, the base current is drawn toward the base electrode, but since the emitter-base junction remains in a forward biased state in the central area of the emitter, a pinch-in effect occurs where the current path remains in the central area only. This concentration of current in the remaining current path leads to a failure.

The above is a brief explanation of secondary breakdown phenomena. While resistance to forward secondary breakdowns decreases as the junction temperature rises, resistance to reverse secondary breakdowns increases at higher junction temperatures. Thus, reverse secondary breakdowns occur due to electrical instability (unevenness), and not due to thermal instability (see Figure 3-51).

Figure 3-51. Breakdown Phenomena During Secondary Breakdowns

![Diagram showing breakdown phenomena during secondary breakdowns](image-url)
3.3.6 \( h_{FE} \) and noise degradation caused by transistor's E-B junction breakdown

When a reverse voltage exceeding \( BVEBO \) is applied between the E (emitter) and B (base) terminals of a transistor, and when a breakdown occurs accordingly, leakage current may increase and \( h_{FE} \) and NF (Noise Factor) may be degraded.

\( h_{FE} \) degradation is thought to be caused by the effects of a new trap center that forms on or near the silicon surface, due to an avalanche breakdown. In other words, an increase in the surface recombination-generation current, which is a component of the transistor's base current, and particularly an increase in recombination current caused by the generation of an R-G center near the surface in the E-B junction's depletion layer (when the collector current is constant and \( h_{FE} = I_C/I_B \)), results in increased \( I_B \) and degradation of \( h_{FE} \).

Another cause is that avalanche breakdowns lead to changes in the surface potential due to the migration of the charge that is thought to exist either between the oxide layer and the silicon boundary or within the oxide layer. However, this has reportedly not been the dominant cause.

To realize the structure of transistors that does not easily lead to \( h_{FE} \) degradation, reduce irregular crystallization during diffusion of impurities and lower the concentration of the base surface. (However, lowering the concentration excessively may result in the occurrence of channels.)

One cause of noise (noise factor) degradation that can be traced to \( h_{FE} \) degradation is an effect of breakdowns whereby the surface recombination-generation current is increased, causing obvious degradation of \( h_{FE} \) in the low-current region and worsening \( h_{FE} \) linearity. This presumption may be true because of the fact that among the input conversion noise components, only the current noise source, \( I_n \) (shot noise), changes while the voltage noise source, \( e_n \) (thermal noise), remains the same.

The following data is provided concerning the amount of fluctuation in noise degradation from these causes, based on the breakdown current value and time, and also concerning the rate of degraded properties recovered by high temperature storage and aging tests.

\(<\text{Degradation of properties by bipolar transistor's E-B junction breakdown}>\)

If a reverse voltage that exceeds the breakdown voltage (\( BVEBO \)) is applied between the bipolar transistor's E and B terminals, a breakdown (avalanche breakdown) occurs, which results in \( h_{FE} \) degradation.

\(<\text{Overview of properties of degraded items}>\)

As is shown in Figure 3-52, transistors with \( h_{FE} \) degradation exhibit an obvious reduction in \( h_{FE} \) in the low-current region. As for the I-D curves between the terminals (breakdown voltage), Figure 3-53 shows normal curves between E and B and between C and B and an abnormal curve between C and E.
h\textsubscript{FE} degradation is thought to be caused by the occurrence of electron traps (parasitic energy levels) on or near the silicon surface, due to an avalanche breakdown. In other words, an increase in the surface recombination-generation current (a component of the transistor's base current), and particularly an increase in recombination current caused by the generation of an R-G center near the surface in the E-B junction's depletion layer (when the collector current is constant and h\textsubscript{FE} = I\textsubscript{C}/I\textsubscript{B}), results in increased I\textsubscript{B} and degradation of h\textsubscript{FE}. Another cause is that avalanche breakdowns lead to changes in the surface potential due to the migration of the charge that is thought to exist either between the oxide layer and the silicon boundary or within the oxide layer. However, this has reportedly not been the dominant cause. In any case, the cause of h\textsubscript{FE} degradation is the increase in the electron trap density near the surface of the E-B region.

Consequently, to make a transistor structure that is less likely to cause h\textsubscript{FE} degradation, the amount of irregular crystallization during injection and diffusion of impurities has to be reduced, and the base concentration has to be lowered.

Reproducibility testing of Compound Semiconductor Devices Division's high-frequency transistor models 2SC5185, 2SC5509, and 2SC5671 provides further information on the results of these causes, namely breakdown.
current values for $h_{FE}$ degradation, dependency on voltage application periods, and recovery from $h_{FE}$ degradation through high-temperature storage.\footnote{Note}

\textbf{Note} Since device structures differ considerably among different device models, the degradation tendency data presented here may not be applicable to other models. Also, the data shown here is based on randomly sampled products, and the range of variation has not been considered.

$h_{FE}$ degradation due to E-B junction breakdown:

(Evaluated products:)

- 2SC5185 (HFT2 process Si Bip.Tr)
- 2SC5509 (UHS0 process Si Bip.Tr)
- 2SC5761 (UHS2 process SiGe HBT)

Figures 3-54 to 3-56 show the amount of $h_{FE}$ degradation that occurs according to the E-B breakdown's current value and the length of time it is applied. Among the aforementioned three transistors, those on which reproducibility tests were performed were two types of silicon bipolar transistors and one type of SiGe hetero bipolar transistor.

In these figures, the breakdown time is shown as accumulated time values, and $h_{FE}$ 1 to $h_{FE}$ 6 are measured in products under the following measurement conditions.

<table>
<thead>
<tr>
<th>$h_{FE}$</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$h_{FE}$ 1</td>
<td>$V_{CE} = 2 \text{ V, } IC = 1 \mu\text{A}$</td>
</tr>
<tr>
<td>$h_{FE}$ 2</td>
<td>$V_{CE} = 2 \text{ V, } IC = 10 \mu\text{A}$</td>
</tr>
<tr>
<td>$h_{FE}$ 3</td>
<td>$V_{CE} = 2 \text{ V, } IC = 100 \mu\text{A}$</td>
</tr>
<tr>
<td>$h_{FE}$ 4</td>
<td>$V_{CE} = 2 \text{ V, } IC = 1 \text{ mA}$</td>
</tr>
<tr>
<td>$h_{FE}$ 5</td>
<td>$V_{CE} = 2 \text{ V, } IC = 5 \text{ mA}$</td>
</tr>
<tr>
<td>$h_{FE}$ 6</td>
<td>$V_{CE} = 2 \text{ V, } IC = 10 \text{ mA}$</td>
</tr>
</tbody>
</table>

<1> $h_{FE}$ degradation according to breakdown time

Figures 3-54 to 3-56 are graphs that show how $h_{FE}$ degrades according to the breakdown time in cases where the breakdown current value is set to 100 $\mu$A, 1 mA, and 10 mA. This $h_{FE}$ degradation is apparent when the breakdown time ranges from approximately 60 to 120 seconds, but degradation slows down afterward. In addition, these graphs show that a higher breakdown current results in more obvious $h_{FE}$ degradation, especially when the IC is in the low-current region.
Figure 3-54  $h_{FE}$ Degradation According to Breakdown Time (2SC5185)

(a) Breakdown current ($I_{EB}$) = 100 $\mu$A

(b) Breakdown current ($I_{EB}$) = 1 mA

(c) Breakdown current ($I_{EB}$) = 10 mA
Figure 3-55. hFE Degradation According to Breakdown Time (2SC5509)

(a) Breakdown current (IEB) = 100 μA
(b) Breakdown current (IEB) = 1 mA
(c) Breakdown current (IEB) = 10 mA
Figure 3-56. $h_{FE}$ Degradation According to Breakdown Time (2SC5761)
h\textsuperscript{2} degradation trends based on various breakdown current values and h\textsubscript{FE} measurement points

Figure 3-57 shows the curves of the amount of breakdown current and reduction in h\textsubscript{FE} (breakdown time = 60 seconds). Although there are slight differences among product models in the h\textsubscript{FE} reduction rates for various breakdown current values, there is a clear trend in which h\textsubscript{FE} reduction increases as the breakdown current value increases. An h\textsubscript{FE} reduction trend becomes apparent once the breakdown current reaches approximately 10 \( \mu \)A. Note that these graphs indicate the h\textsubscript{FE}’s measurement point dependency in the h\textsubscript{FE} reduction trends, they also indicate that h\textsubscript{FE} reduction or h\textsubscript{FE} retention rate appears more obvious in all product models in the region where the measurement conditions of collector current is small.
Figure 3-57. Breakdown Current Dependency of $h_{FE}$ Reduction (Retention) Rate

(a) 2SC5185

(b) 2SC5509

(c) 2SC5761
The above test results show that $h_{FE}$ degradation occurs when a breakdown current flows between the emitter and base in Si bipolar transistors. In these cases, the $h_{FE}$ reduction trend is more apparent as the breakdown current value increases, and in the region where the measurement conditions of collector current is small.

<3> High temperature storage for recovery of $h_{FE}$ degradation

Figure 3-58 shows how $h_{FE}$ degrades when transistors with $h_{FE}$ degradation are stored at high temperatures. In these cases, the initial values (values prior to the occurrence of breakdowns) are presumed to be 100%.
Figure 3-58. $h_{FE}$ Recovery Trends During High Temperature Storage (breakdown current = 100 $\mu$A)

(a) 2SC5185

(b) 2SC5509

(c) 2SC5761
The following conclusions can be drawn based on the results described in <1> to <3> above.

(1) $h_{FE}$ degradation is most obvious at the moment of breakdown, and it progresses only slightly thereafter.
(2) $h_{FE}$ degradation is much more dependent on the breakdown current than on the breakdown time.
(3) $h_{FE}$ degradation is more apparent in low current regions.
(4) $h_{FE}$ degradation can be recovered somewhat through high temperature storage, so it is not permanent degradation. However, it is rarely recovered to its initial level.

3.3.7 Catastrophic optical damage (COD) in laser diodes

In the case of many laser diodes that output visible light, when the optical output is boosted, optical output suddenly drops as shown in Figure 3-59, the active regions on the laser diode’s facets become damaged, and some of this damage is irreversible. This phenomenon is called COD (Catastrophic Optical Damage) and occurs when the optical output density at the mirror facet, under CW operation, reaches approximately $1 \times 10^{4.6}$ (W/cm$^2$).

COD damage is caused when the AlGaAs active layer near mirror facets become laser light absorption regions. There are many levels on the crystal surfaces of GaAs or AlGaAs materials, which result in nonradiative recombination.

Carriers injected to the active layer near mirror facets are lost through repeated recombination, and the density of injected carriers in these regions is low when compared to the central part of the stripe. As a result, when the light wave energy density in the active layer is considered from the perspective of laser light gain or absorption rates, the mirror facets become absorption regions (see Figure 3-60). When the optical output density is increased, the absorption region absorbs more optical output energy, and local heat generation at the mirror facets (i.e., absorption regions) raises the temperature, which reduces the band gap. Consequently, the mirror facets’ optical output absorption rate further increases, which spurs further absorption and heat generation. Thus, while the laser diode is operating, this vicious cycle is repeated until the temperature near the mirror facets reaches the melting point, causing damage.

Figure 3-61 shows an example consisting of an image of an infrared light that is at the front facet of a visible wavelength laser diode suffering from COD. In this image, an LED is lit under adequate conditions. In most cases, the active layer’s NFP (Near Field Pattern) has a double hump shape.
Figure 3-61. IR Image (NFP) of Visible Wavelength Laser Diode Suffering from COD

- Near field pattern (NFP)
- Distribution of optical output intensity
CHAPTER 4 FAILURE ANALYSIS

4.1 About Failure Analysis

4.1.1 Failure analysis steps

4.1.2 Use of CAD data for failure analysis

4.2 Principal Analytical Methods

4.2.1 SAT

4.2.2 SEM (Scanning Electron Microscopy) and EPMA (Electron Probe Micro Analysis)

4.2.3 EB tester analysis

4.2.4 Photoemission microscopic analysis

4.2.5 OBIRCH (Optical Beam Induced Resistance Change) method

4.2.6 Failure analysis techniques that use Iddq abnormality images

4.2.7 SIMS (Secondary Ion Mass Spectrometry)

4.2.8 AES (Auger Electron Spectroscopy)

4.2.9 FT-IR (Fourier Transform Infrared Spectroscopy)

4.2.10 TEM (Transmission Electron Microscopy)

4.3 Processing Technology for Analysis

4.3.1 General

4.3.2 FIB (Focused Ion Beam)

4.3.3 Sublimation processing laser

4.3.4 RIE (Reactive Ion Etching)

4.4 List of Failure Analysis Devices

4.4.1 Devices used for visual inspection and operation analysis

4.4.2 Devices used for analytical research
CHAPTER 4 FAILURE ANALYSIS

4.1 About Failure Analysis

4.1.1 Failure analysis steps

One of the important parts of failure analysis is determining “to which extent can failure sites be identified while keeping the electrical circuits and abnormalities as they are?” Today’s analytical tools can analyze a device’s operating conditions using non-contact and non-destructive methods. The EBIC and OBIC are examples of tools used to visually analyze a device’s operating conditions. To visually check the recombination or excitation of electrons on the junction surface, there are two methods:

1. Apply a current to the target device when an emission microscope is used.
2. Apply an electron or laser beam to the target device when EBIC or OBIC is used.

Meanwhile, ongoing IC development trends include miniaturization, multilayer interconnection structures, larger-scale integration, faster processing speed, and hybridization. All of these trends pose challenges for failure analysis. Developers of processing technologies must consider ways to enable non-destructive analysis of failures and abnormal conditions in electrical circuits. New devices such as laser devices, FIB (Focused Ion Beam) devices, and FLB (Focused Laser Beam) devices have been developed to implement these types of processing technologies.

For some logic ICs, software-based failure analysis tools have been developed, and these tools are able to identify failure sites without performing physical analyses. A typical method is to apply a reversed logic to the inside of the IC, based on data of the abnormal logic output from output terminals of the device. Another method is to use Iddq abnormalities (power supply current abnormalities during the static state) and CAD data to identify the sites where the current abnormalities have occurred.

Figure 4-1 outlines the steps generally followed during failure analysis. The key is to clarify the cause-and-effect relationships at each step while working toward the next step. Failure analysis is not completed until the results of analysis can be used to explain the abnormal operations that are occurring in the electrical circuits.
Figure 4-1. Failure Analysis Steps

External view inspection

Appraisal of failure

Measurement of performance characteristics

X-ray observation

Unpacking

Observation of chip’s surface

Identification of failure site

Physiochemical analysis and structural analysis

Confirmation, verification, and proposed responses to failure mechanisms and causes
(1) Understanding failure conditions
It is important to gain an understanding of the samples that are collected when a failure occurs and also the conditions under which the failure occurred. Environmental factors (temperature, humidity, operating voltage, mounting condition at the time of the failure, etc.) are particularly important. Such data is essential for evaluating failures when analyzing samples.

(2) Visual inspection
When samples are received, they are visually inspected for cracks, burn marks, bent external pins, etc.

(3) Analysis of electrical operations
An IC tester is used to check the device’s operating status (use the test programs for outgoing inspection and evaluation). Check high-frequency characteristics, DC characteristics, temperature characteristics, linearity, etc.

(4) Stress testing
When the failure cannot be confirmed by previous tests and analyses, stress is applied with reference to the information on failure occurrence conditions to check whether or not the failure can be reproduced.

(5) Non-destructive analysis
Check devices that have been targeted for analysis of electrical operations. In particular, DC failures can be caused by abnormalities of not only internal elements but also package, so a microscope should be used for pattern inspections (shorted pin connections, cracks between pins, etc.). X-rays are used to observe internal conditions, such as wire patterns. In addition, ultrasonic probes are used to check adhesion strength between the package and the internal elements and to check for micro-cracks in the package.

(6) Semi-destructive analysis
First, open the package to expose the surfaces of the inner elements. Use a mechanical method to open ceramic or metal packages. For plastic packages, use chemicals to etch the plastic and expose the surfaces of the inner elements. Use an optical microscope to inspect these surfaces of the elements. During the external view inspection, any abnormal sites are cross-checked against the corresponding electrical characteristics. Whenever necessary, use other tools such as a photo emission microscope for this analysis.

(7) Destructive analysis
During destructive analysis, the specimen is inspected for failure sites as it is etched away layer by layer, from the passivation layer to wiring and bonding layers, etc. The specimen is cut (using an FIB) for inspection and elemental analysis. If analysis of diffusion-related abnormalities is required, device-specific characteristics (Tr characteristics, leakage resistance, etc.) are checked. Mechanical probers are an effective tool for this. Also, an FLB is used to check characteristics based on electrode formation (probing pads). In addition, Compound Semiconductor Devices Division uses destructive analysis technologies such as lasers, FIBs, and RIEs. For example, when analyzing a multi-layer structure, make a hole in the top wiring layer to expose lower-layer circuit patterns. In addition, change any interconnections in order to focus on a particular target function.
4.1.2 Use of CAD data for failure analysis

While greater design efficiency is being demanded against a backdrop of semiconductor device design trends such as higher integration, multilayer design, and flatter design, there are also demands for shorter failure analysis periods and a customer service-oriented emphasis on faster identification of the causes of failures. Although various types of analytical tools and equipment can be used to efficiently and comprehensively analyze the complex behavior of semiconductor device chips, use of CAD data is also important as an analytical approach that provides one of the fastest turnaround times.

Since CAD data includes a variety of design-related data, it is important to select only the data that is required for an appropriate analysis. Some proficiency with using CAD systems is desirable, since such data can be found most efficiently within CAD data files and amidst other existing collections of data. Described below is a “CAD navigation system” that helps to efficiently find correspondences between terms on a circuit drawing and items in the actual circuit layout when studying failure sites observed via an electron beam tester or FIB device. Figure 4-2 shows an outline of CAD navigation.

Figure 4-2. Outline of CAD Navigation

CAD navigation includes a layout display function and a function for locking positions corresponding to physical coordinates. Layout display methods are divided into three categories: (1) layout display only, (2) layout display with netlist display, and (3) circuit diagram (schematic) display linked to layout display.
(1) **Position locking with layout display**

The basic mechanism of CAD navigation is a mechanism, which displays layout and locks positions being observed using inspection equipment such as EB tester and FIB devices. Positions within wiring diagrams and other graphic layout information can be selected and highlighted (such as by clicking a mouse) to make them more visible and easier to identify, which is very useful when tracing interconnect patterns. Position locking methods differ among different equipment brands and manufacturers: some lock positions are displayed in separate windows showing the layout or a SEM image, while others present a layout display as an overlay on a SEM image or other image.

Generally, the separate-window method is used for items that are particularly significant, such as when displaying the shading within an image, while the image overlay method is more suitable for accurately determining positions. The only type of files needed to provide data from layout displays are chip layout data files (files in the industry-standard GDS II format are supported). This method enables displays to be called up simply by defining the target layer and data.

(2) **Position locking using links between netlist display and layout display**

This is a mechanism for drawing correspondences between layout sites and circuit (netlist) drawing numbers by linking layout displays with netlist displays. When graphic data in a layout drawing is highlighted (such as by clicking the mouse), the corresponding circuit drawing number from the netlist is also highlighted. This linking function works in both directions, so that highlighting a circuit drawing number in the netlist will cause the corresponding graphic data to be highlighted in a layout drawing. This greatly improves researchers’ ability to confirm circuit sites using only layout displays. Although netlist linking requires both layout data and netlist data, the netlist data format can be either the generally used EDIF format or the SPICE format. Unlike when using only layout displays, the netlist linking method requires not only layers but also components and blocks to be defined in detail.

(3) **Position locking using links between circuit (schematic) drawing display and layout display**

This is a mechanism for drawing correspondences between layout sites and circuit (schematic) drawing numbers by linking layout displays with circuit drawing displays. After highlighting (such as by clicking the mouse) graphic data in a layout drawing, the corresponding section from the corresponding circuit drawing is also highlighted. This linking function works in both directions, so that highlighting a section of a circuit drawing will cause the corresponding graphic data to be highlighted in a layout drawing. This method is the best for enabling researchers to confirm circuit sites in circuit drawings without having to be familiar with the format of netlists. Although schematic linking requires both layout data and schematic data, the data format can be either the generally used EDIF format or the SPICE format. As with netlist linking, this method requires not only layers but also components and blocks to be defined in detail and it requires greater consistency between the circuit drawings and layout displays.

As noted above, there are several methods being used for CAD navigation. From the perspective of circuit diagram recognition functions, the “schematic linking” method is best, but it involves rather complicated setup procedures. By contrast, the “layout display only” method provides the least effective circuit diagram recognition functions but has very simple setup procedures. Therefore, it is important to select the method that best suits your use objectives. Generally, the schematic linking method and the netlist linking method are most effective when seeking correspondences between physical sites and circuits when circuit-related failure causes are being investigated, while the layout display position locking method is adequate when merely looking for physical sites, such as in FIB images of lower-layer interconnects or section views. Photo 4-1 shows an example of how the layout-netlist linking can be used with EB tester results. The netlist display is in the upper left section, the SEM image is in the lower left section, and the layout display is in the lower right section. A display of waveform data is shown in the upper right section.
Photo 4-1. CAD Navigation with EB Tester
4.2 Principal Analytical Methods

4.2.1 SAT

[Objective]
To use reflected ultrasound waves as a means of nondestructive observation of conditions (presence/absence of cracks or cavities) in materials.

[Principle]
Figure 4-3 shows a configuration diagram of this device and describes how it produces images. A repeated pulse voltage is applied to an ultrasonic sensor assembly that includes an ultrasonic oscillator and an acoustic lens. Ultrasound waves that are emitted from the ultrasonic sensor are reflected from the specimen’s surface (including any surface defects) and return to the ultrasonic sensor. A piezoelectric element outputs the reflected ultrasound waves as voltage values to a receiver. The receiver amplifies the weak signals that represent raw data and then outputs the signals to a detector. The detector outputs DC voltage values corresponding to peak values for a section that will be converted into an image, such as by using a detection circuit (gate circuit) to process the ultrasound waves that were reflected from the surface of a bonding layer. Meanwhile, the ultrasonic sensor is attached to a scanner which outlines (via a controller) the horizontal or vertical plane of the specimen. The A-D conversion of the above-mentioned DC voltage values is performed using the specified measurement pitch during the scanning operation, after which the converted values are processed and stored to display addresses corresponding to their original X/Y coordinates so as to provide a real-time display of scanned images, such as the above-mentioned bonding layer surface.

[Specific applications]
- Evaluation of adhesion strength between silicon chip and mold resin (see Photos 4-2 and 4-3)
- Evaluation of adhesion strength between lead frame and mold resin
- Die bonding evaluation
- Observation of voids in mold resin
- Observation of package cracking
- Observation of chip cracking
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Figure 4-3. Configuration Diagram of SAT Device

Photo 4-2. No Abnormalities

Photo 4-3. Peeling at Chip’s Corners
4.2.2 SEM (Scanning Electron Microscopy) and EPMA (Electron Probe Micro Analysis)

[Objective]
The chief objectives are to observe the condition (smoothness, etc.) of solid surfaces and to analyze the surfaces' constituent materials.

[Function]
SEM allows researchers to easily observe three-dimensional shapes at various depths of focus and under high magnification. SEMs enable observation of defects, detailed structures, and tiny impurities that are too small to be observed using optical microscopes. An EPMA enables researchers to learn more about the constituent materials of solid surfaces (qualities of elements existing at a specified site, quantitative analysis, and distribution of specified elements).

[Principle]
An electron beam that is output from an electron gun passes through several electron lenses to become finely focused as it irradiates the specimen. The size of the electron beam can be adjusted to between several dozen Å and several dozen μm to suit the object being measured. As shown in Figure 4-4, secondary electrons, back-scattered electrons, and characteristic X-rays are among the objects that are reflected from the surface of the specimen. The SEM's secondary electron images are synchronized with the electron beam scanning of the specimen surface and the intensity values of secondary electrons are converted to luminance values in the monitor display. The luminance values of secondary electrons differ according to the surface smoothness, constituent elements, and surface potential. Such changes can be observed in the secondary electron images.

Figure 4-4. Electrons and X Rays Reflected from Surface of Specimen
As can be seen in the basic EPMA configuration diagram shown in Figure 4-5, an X-ray detector has been attached to the SEM unit. Since characteristic X-rays have specific energy values corresponding to specific constituent elements, measuring these energy values enables researchers to identify types of elements present on the target surface. Like SEM units, EPMA units synchronize electron beam scanning of the target surface. The characteristic X-rays of a specified element that have been detected are displayed on the monitor as numerous dots that together form a “map” showing the specified element's distribution (this is called “elemental mapping”). Researchers can also determine the concentration of the specified element by comparing the density of a pre-measured standard specimen with the specimen.

**Figure 4-5. Basic Configuration of XMA**

[Analysis example]

Photo 4-4 shows the mapping of various elements’ distribution in a defective area in a crystal glass specimen. The maps show that the defective areas contain extra amounts of silicon and aluminum. When the back-scattered electrons are detected and displayed, the condition of the surface is displayed much more clearly than in the display of mapped secondary electrons.
Photo 4-4. Scan Images of Defective Area in Crystal Glass (X200)

Surface image from reflected electrons

SiKα image

FeKα image

AlKα image

Reference
- “X-ray micro analyzer” I. Uchiyama et al. (Japanese version only)
4.2.3 EB tester analysis

[Objective]
An electron beam is used for detecting logical information (potential contrast images, logical operation waveforms) on the IC device in the vacuum chamber, driven by an IC tester (see Figure 4-6).

[Function]
- Potential contrast images: A potential contrast image corresponding to the potential differences among the wirings can be viewed (black = high potential, white = low potential) (see Photo 4-5).
- Logic operation waveform (potential waveform): Enables the observation of the logic states of any internal wiring in chronological order according to the input pattern (see Figure 4-8).

Using the functional features described above, Compound Semiconductor Devices Division has developed new analytical methods that are easy-to-use and efficient. One of these methods is the CGFI (Continuous Gated Fault Imaging) method, which is used to quickly obtain potential contrast images having high S/N ratios. Another method is the AFI (Activated Fault Imaging) method that can blinkedly highlight the fault signal propagated portions, which guide the operator to the failing cell location.

- CGFI method: A continuously emitted primary electron beam is used to effectively eliminate charge-up phenomena and prolonged gate pulses generate rich signal so that high-contrast potential contrast images can be quickly obtained.
- AFI method: Only the wiring through which failure signals propagate can be blinked and monitored by using the CGFI method on marginal defective ICs, such as voltage margin, while switching acceptable product condition and defective product condition at high speeds (see Photo 4-6).

[Principle]
When electrons emitted from an electron gun are irradiated onto the surface of an IC, secondary electrons are generated. The quantity of secondary electrons is a constant, but their energy distribution varies according to the potential, so logic states can be inferred once the energy distribution has been identified. Relative to the ground potential, the curve on the left in the figure represents the energy distribution for a positive potential and the curve that is shifted to the right represents the energy distribution for a negative potential. If a potential barrier is attached between the IC and the secondary electron detector, only those electrons that have enough energy to cross the barrier reach the detector. This means that the IC’s potentials can be compared relatively based on a comparison of detected secondary electrons (see Figure 4-7).
Figure 4-6. Outline Drawing of SEM System

![Outline Drawing of SEM System](image)

Electron gun
Condenser lens
Pulse electron beam
Objective lens

IC tester

Pulse electron beam generator

Signal processor

DUT (Device under test) board stage

Figure 4-7. Energy Distribution of Secondary Electrons

Energy distribution of secondary electrons generated from IC

![Energy Distribution of Secondary Electrons](image)

Secondary electrons that have crossed the grid

Quantity (Q) of secondary electrons as determined by integrator-type detector

\[ Q = \int_{W_o}^{\infty} N(W) \, dW \]

Q (High) < Q (Low) enables relative comparisons
Figure 4-8. Logical Operation Waveforms

Changes in logical operation waveforms in CMOS circuit
IN, OUT: Observed on bonding pad
P1, P2: Observed on passivation layer
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Photo 4-5. Potential Contrast Images

Potential contrast image of nondefective specimen

Potential contrast image of defective specimen

Differential image

Photo 4-6. AFI Image

Failure site (wire)

References

- Hanagama, Nakamura, Nikawa, Tsujiide, Noguchi, Kato, Okane “Reduction of Effect of Charge up by High-speed Potential Distribution Image Capture” 125th research conference of 132nd committee meeting of EB testing symposium pp.131 to 136 (Japanese version only)
4.2.4 Photoemission microscopic analysis

[Objective]
This device detects photoemission phenomena that occur when a voltage is applied to an IC. A highly sensitive detection device detects small photoemissions and stores images of them that can be output via a processor and displayed on a monitor.

[Function]
(1) Detection of sites where hot carriers occur
(2) Detection of dielectric layer failure sites (shorting, leakage)
(3) Detection of pn junction failure sites (shorting, leakage)
(4) Detection of photoemissions due recombination of minority carriers when pn junction is forward biased
(5) Detection of latchup sites
(6) Observation of photoemissions during a function's operating state (when linked to IC tester)
(7) Observation of photoemissions from rear surface
(8) Spectral analysis of photoemissions

[Principle]
When junction leakage or dielectric layer defect occurs, application of a voltage will cause an electric field to become concentrated at the failure site, which generates hot carriers. A detector is used to detect the photons that are discharged when recombination occurs. This detector includes a highly sensitive near-infrared camera with a built-in image intensifier as well as a high-sensitivity high-resolution cooled CCD camera. In addition to being sensitive enough to detect individual photons, the near-infrared camera provides a gate function for capturing rapid transient phenomena and a function that enables real-time observation of changes in photoemission. The CCD camera is sensitive across a wide range of wavelengths (from 300 to 1100 nm) and is able to provide high-resolution pattern images. Very weak photons that are detected by this detector are treated as secondary photon images. By outputting these images to a monitor as overlay images on pattern images, it becomes possible to specify the photoemission sites. (See Figure 4-9 and Photo 4-7.)
Figure 4-9. Outline Drawing of Photoemission Microscope System (When Linked to IC Tester)

Photo 4-7. Photon Observation Examples

Light emission in forward direction of C-B junction

Light emission in reverse direction of C-B junction
4.2.5 OBIRCH (Optical Beam Induced Resistance Change) method

[Objective]
This method is basically used for non-contact analysis of interconnects on IC chips, but it is sometimes used to detect substrate-related failures, depending on the causes of those failures.

[Function]
There are two different functions. These functions can be used not only on the chip's front side but from the rear surface as well.

(1) Detection of current path in devices with defects which cause power supply current increase, I/O leakage current increase, etc.
   Images of current flowing as DC current can be observed.

(2) Detection of abnormalities including voids, silicon precipitation, and parasitic high-resistance layers
   This method enables detection not only of voids on metal surfaces but also voids and silicon precipitation that are buried in the metal layer. It can also detect voids in and around vias, as well as very thin (a few nm) high-resistance layers that are formed at the bottoms of vias.

[Principle]
The specimen is heated by a laser beam, after which the current changes produced by this event are observed and the two functions described above can be used.

A detailed description is given as follows. While a constant voltage is being applied to the specimen, a laser beam is used to scan the area being observed while power supply current changes in the scanned area are displayed on the monitor as changes in brightness. The displayed brightness increases and decreases as the current increases and decreases. When the laser beam irradiates the metal, the metal temperature rises and the resistance value of the metal raises. As a result, a decrease in current is observed. This enables the interconnections through which the current flows to be shown as a dark area in contrast to surrounding areas.

Since the momentary temperature rise that occurs when the laser beam irradiates a site having defects (voids, silicon precipitation, etc.) that degrade thermal conduction in the interconnection material is greater than the momentary temperature rise that occurs when the laser beam irradiates a site where no such defects are present, the greater temperature rise causes a greater increase in resistance and a greater reduction in current, so that the defect site is shown as a dark image. The parasitic high-resistance layers that occur at the bottoms of vias often have negative temperature characteristics. Consequently, when the laser beam irradiates one of these layers, resistance decreases and a bright image is displayed corresponding to that site.

An ordinary OBIC (Optical Beam Induced Current) device is used to implement the OBIRCH method. However, the sensitivity must be higher than that required for detecting ordinary OBIC signals. Figure 4-10 shows a configuration example for this system. This system is available in two types: a type that uses a visible laser (wavelength: 632.8 nm) and a type that uses a near-infrared laser (wavelength: 1300 nm). Although higher spatial resolution can be obtained from the visible laser type, to make this system suitable for actual devices other than TEG (Test Element Group), some way must be devised. If the OBIC current is allowed to flow as a power supply current, the OBIC signals will interfere with the OBIRCH signals and will prevent OBIRCH images from being displayed. Devising a way to prevent OBIC current flow is very difficult, however. If a near-infrared laser (wavelength: 1300 nm) is used instead, no OBIC signals will generated, which makes the system easily suitable for actual devices. Using a near-infrared laser also facilitates observations from the rear side of the chip: even if the chip is not a thin chip, about half of the laser beam will still reach the interconnections.
The surface of the specimen is scanned by a He-Ne laser (632.8 nm, 2 mW to 20 mW) that has been set to its minimum beam diameter (0.43 μm). In digital terms, the scan width is 512 × 512 pixels, and the dwell period for each pixel is about 2 μs, so that each scan takes about 0.5 seconds. Usually, an integration factor of 10 to 20 times is required to obtain a high-quality image. One step of a digital scan at maximum magnification (3,600, visual field: 35 μm × 35 μm) is approximately 0.068 μm. There are three types of current change detectors: one has a maximum conduction capacity of 200 mA and a current change detection resolution of 400 nA (when the S/N ratio is 2), the second has a maximum conduction capacity of 100 mA and a current change detection resolution of 1 nA, and the third has a maximum conduction capacity of 20 mA and a current change detection resolution of 100 pA.

The infrared laser devices use a laser diode (1300 nm, 500 mW) that emits beams that can be focused to diameters ranging from 1.87 μm (theoretically, 83% of the total energy falls within this range when the visual field is 112 × 112 μm) to 21.1 μm (when the visual field is 5 × 5 mm). Scanning is an analog operation requiring about 5 seconds per scan. In cases where the S/N must be raised, an integration factor of up to 16 times is used. Images are captured as 512 × 512 pixels.

Figure 4-10. Configuration of Required to Implement OBIRCH

![Configuration Diagram]
(1) Detection of current path in device with power supply current defect

Figure 4-11 shows an example of a current path that was detected on the rear side of a chip. A near infrared laser system was used in this case. After the current path was detected within a wide visual field (5 mm x 5 mm), the device was set to a higher magnification to check the defect site. In this example, the wiring width is approximately 1.5 $\mu$m and the current that flows on the wiring has a value of about 1 mA. Note that although the beam diameter is approximately 20 $\mu$m when scanning the 5 mm x 5 mm area, it is still possible to observe current flowing on a line that is about 1.5 $\mu$m wide. There have also been examples in which current flowing on a line that is about 0.4 $\mu$m wide has been observed (See reference below).

Figure 4-11. Current Path Observation Example
(2) Detection of defects (voids, silicon precipitation, parasitic high resistance layers, etc.)

Figure 4-12 shows an example in which a visible laser system was able to detect voids created by electromigration.

Figure 4-12. Example of Detected Voids in Via

References

• The following three references provide general descriptions of functions other than detection of high-resistance layers.


3) Nikawa, K. and S. Inoue, “Use of Infrared Laser Beams to Analyze Failure Sites in VLSIs,” collected papers for 26th Reliability and maintainability symposium of Union of Japanese Scientists and Engineers, pp.77 to 82 (1996) (Japanese version only)

• The following reference provides a detailed description of how near infrared radiation is used.


• The document below contains recent examples of the use of near infrared radiation. It also describes high resistance layer detection for which the radiation is used. Other application examples using the same equipment and the operation principles are not described in this document.

4.2.6 Failure analysis techniques that use Iddq abnormality images

[Objective]
The objective is to use these techniques to investigate IC power supply current-related phenomena in order to select defective products and localize fault sites without logic operation error. Compound Semiconductor Devices Division has developed testing and failure analysis techniques by these phenomena.

[Function]
These techniques can be applied to localize the fault portion and substituted to IC testing and accelerated testing. A detailed description is provided below.

[Principle]
Iddq (quiescent VDD supply current) phenomenon is a signal to present a physical damage in an IC circuit (see Figure 4-13). While test vectors are applied to input, Iddq values are measured for each vector and the abnormal signals are detected.

* Testing
Iddq test which is added to logical operation tests is applied to detect the fault of modes overlooked by logical operation tests alone and to compensate the fault detection rate logical operational testability. With increasingly high integration scales, Iddq test has been indispensable test method.
Compound Semiconductor Devices Division has been involved in Iddq tests from early on. Today, Compound Semiconductor Devices Division is working to develop new applications for Iddq testing. Figure 4-14 contains a graph that indicates the general relation between devices with logical operation defects and items with Iddq defects. Note that while almost all logical operational errors are detected by Iddq tests, abnormal Iddq not always be detected by operation tests. Compound Semiconductor Devices Division has been established the efficient Iddq testing methods by studying characteristics of vector composition and by calculating toggle ratio of all test vectors.
**Application to accelerated testing**

An Iddq test has been studied to eliminate devices with early failures. Conventionally, such devices are screened out by the screening process. The basic reason for this application of Iddq testing is that early failure devices detected under the accelerated tests (with higher temperature and voltage condition), have a latent fault mode and denote the significant difference of Iddq values among the sound devices.

**Failure analysis (application to physical analysis)**

These techniques are finding greater use in failure analysis as techniques for detecting physical failures. Because Iddq failure sites bring abnormal photon, abnormal heating, and abnormal current, and these phenomena make it easy to detect leakage sites. Emission microscopes (see 4.2.4 above) are typically used to detect photons, while the OBIRCH method is used as a visual detection method for abnormal current paths. Improvements have been made in all of these methods, which have raised their analytical precision. Accordingly, Compound Semiconductor Devices Division’s failure analysis flow starts with detection of Iddq defects before going on to more detailed analyses.

**Failure analysis (localization of failure sites through CAD tools)**

Advances in layout pattern configurations, package structures, and multilayer interconnect structures have made it more difficult to expose IC surfaces in order to detect failure sites. Consequently, there has been an urgent need for failure site detection methods that do not rely on physical analysis. In response to this need, Compound Semiconductor Devices Division has developed a failure site detection method that uses Iddq failure phenomena in a CAD application. This method includes algorithms specifically designed for detecting failure sites based on CAD (design) data and test vector data related to abnormal Iddq. Currently, Compound Semiconductor Devices Division is preparing this method for practical use (see Figure 4-15).
Figure 4-15. Failure Site Detection Method Using CAD Data and Test Vector Data for Abnormal Iddq

1. Test vectors for FT
2. Circuit connection data
3. Logic simulation
4. Dump processing to extract internal circuit nodes
5. Measurement of Iddq values
6. Extraction of input logic to each block for each test vector
7. Test vector number extraction from abnormal Iddq
8. Processing
9. Extraction of failure blocks

References
- Sanada, Itou, Numajiri, Suzuki and Sasaki, “Methods for Evaluation and Elimination of Iddq Abnormalities in CMOS Logic Circuits,” 125th research conference of 132nd committee meeting of LSI testing symposium pp.7 to 12, Dec.1993 (Japanese version only)
- M. Sanada, “A CAD-Based Approach to Failure Diagnosis of CMOS LSI’s Using Abnormal Iddq” 14th IEEE VLSI Test Symposium, pp186 to 191, April/1996
4. 2. 7 SIMS (Secondary Ion Mass Spectrometry)

[Objective]
To measure the depthwise concentration distribution of impurities beneath the surface of a solid specimen, or the depthwise composition distribution of a semiconductor material.

[Function]
Able to measure elements ranging from hydrogen to uranium, as well as their isotopes
Wide dynamic range (approximately 6 digits, from ppm to ppb)
High detection sensitivity (dopant in Si: $10^{14}$ cm$^{-3}$)
Depth profile (depth resolution: up to several nm)
Able to analyze solid specimens (metals, semiconductors, insulators)

[Principles]
A specimen is irradiated with an ion beam (from several hundred eV to several hundred keV), and sputtering is performed. At the same time, secondary ions are accelerated and captured within a specified electric field. Then, they are detected by mass spectrometry (Figure 4-16).

[Case study]
Figure 4-17 shows an example of a SiGe transistor electrode measured depthwise. Both depthwise composition distribution and density are detected.
Figure 4-16. Double Focusing Secondary Ion Mass Spectrometer

Figure 4-17. Example of SiGe Transistor Electrode Analysis
4.2.8 AES (Auger Electron Spectroscopy)

[Objective]
AES (Auger Electron Spectroscopy) is a method for analyzing the top surface layer of very small areas. This method is used to examine the constituent materials in thin films, surface/boundary structures, diffusion of elements, particle components, residual dielectric layers on bonding pads, discoloration of leads, and impurities found between layers.

[Function]
- Can detect all atoms except H and He.
- Detection limit ranges from 1 to 0.1 A.C. % (atomic percent concentration).
- Can analyze thin-film surfaces (to 5 nm depth).
- Can analyze extremely small areas by focusing electron beam (the most recent equipment model has a minimum electron beam diameter of approximately 20 nm).
- Uses sputter etching to enable measurement of component distribution in depth direction.
- Can use electron beam to measure planar distribution or linear distribution of target elements.
- In some cases, atomic combinations can be inferred from Auger peak formations and energy shifts.

[Principle]
AES uses the Auger electrons that are discharged when a specimen is irradiated with an electron beam. Electron energy values can be used to identify or quantitatively analyze chemical elements.
Auger electrons are discharged via the following process, which is called the Auger transition process.
(1) An electron beam ionizes inner-shell electrons from atoms in the specimen, which generates core holes.
(2) The core holes absorb outer-shell electrons. When that happens, energy equivalent to the energy differential between the core hole and the outer-shell electron is discharged.
(3) The discharged energy excites another outer-shell electron, causing it to be discharged from its atom. This discharged electron is called an Auger electron.
The energy of Auger electrons being measured ranges from 50 to 2000 eV. Auger electrons that are able to escape the specimen occur at a depth of about 5 nm from the surface. To detect these Auger electrons, AES uses an ultra-sensitive analytical method for the top surface.

[Example of analysis]
Figure 4-18 shows a depth profile measured using AES and sputter etching from above the gate after the gate wiring has been mechanically ground until the polysilicon is exposed. In this example, a gate oxidation layer having a depth of 11 nm was detected.
Figure 4-18. Depth Profile of Gate Oxidation Layer

![Graph showing depth profile of gate oxidation layer with sputter time (m) on the x-axis and strength (kcps) on the y-axis. The graph indicates the presence of gate oxidation layer with distinct peaks and troughs corresponding to oxygen (O) and silicon (Si) concentrations.]
4.2.9 FT-IR (Fourier Transform Infrared Spectroscopy)

[Objective]
FT-IR (Fourier Transform Infrared Spectroscopy) is mainly suited for analysis of high-polymer substances such as rubber, paper, plastic, fibers, cloths, and adhesives. For semiconductors, this method is used to analyze impurities that are inside or on top of the silicon wafer.

[Function]
Infrared spectroscopy is an indispensable method for analyzing the structure of organic compounds. This technology is particularly noted for its ability to obtain motion-related information, such as elasticity or deformation vibration of the polymer functional group.

The generally used type of FT-IR device is able to very quickly make highly sensitive measurements of the spectral phenomena in the target area and to obtain high-resolution spectral data for highly precise wavelength values. It can also measure specimens that have very little mass or low permeability.

[Principle]
When a specimen is irradiated with an infrared beam, light is absorbed selectively (only in certain wavelengths). An infrared absorption spectrum can be obtained by recording the strength of an infrared beam that has permeated the target substance as the vertical axis and the infrared wavelength as the horizontal axis. Like fingerprints, each infrared absorption spectrum is unique to the measured substance, which makes it very useful as a means of identifying substances. Since the wavelengths around which certain types of component structures are absorbed are already known, this technology enables researchers to use spectrum data to determine the chemical structure of previously unknown substances.

As shown in Figure 4-19, an infrared beam is emitted from a light source and strikes a semi-transparent mirror (a beam splitter), where it is split in two directions. These two beams of infrared light are reflected by mirrors (a fixed mirror and a moveable mirror) and meet again at the semi-transparent mirror. While these measurements are being taken, the moveable mirror is moved back and forth so that a different optical path results in comparison to the fixed mirror. The differential between infrared beam’s two optical paths is used as function for creating an interferogram. The interferogram are again split in two directions. One of the interferogram returns to the light source and the other penetrates the specimen and reaches the detector. At the detector, the electrical signals corresponding to the interferogram undergo Fourier transform processing via a computer to produce an infrared spectrum. The usual measurement method starts by measuring the background spectrum before setting up the specimen, then the specimen is set and the spectrum is again measured. The specimen's infrared spectrum is obtained by calculations based on a comparison of the two measured spectra.

The main analytical methods related to FT-IR technology include the thin-film transmission method, attenuated total reflectance (ATR) method, liquid ATR method, diffusion reflectance method, infrared microscopy method, GCF/FT-IR method, and photo-acoustic spectroscopy.

The following are brief descriptions of two of these methods that are used relatively often: the attenuated total reflectance (ATR) method and the infrared microscopy method.

- Attenuated total reflectance (ATR) method
  The purpose of this method is to analyze the surface of the specimen. It is used for thin-film analysis and for cases in which the specimen’s absorption strength is too strong to disable a good spectrum to be obtained via the thin-film permeation method (due to saturation).

- Infrared microscopy method
  An infrared microscope is used to perform transmission and reflection measurements of a small area (up to 20 μm wide). This method is used to identify impurities that are introduced during production processes. In such cases, measurements can be made with almost no preprocessing of the specimen required.
Figure 4-19. Configuration of FT-IR System

Light source
Semi-transparent mirror
Fixed mirror
Movable mirror
Michaelson interferometer

Laser source
Specimen
Detector
[Example of analysis]

1) Evaluation of Si-H in structure of SOG layer

Figure 4-20 shows the result of a study of the optimum baking temperature of an SOG (Spin On Glass) layer. This study used FT-IR technology to measure the Si-H reduction trend that occurs when the SOG layer is under bake conditions. Temperature changes at the peak elasticity and vibration values for Si-H are shown in the figure. It is evident that higher baking temperatures result in fewer Si-H compounds and lower peak strength values.

Figure 4-20. Temperature Changes at Peak Elasticity and Vibration Values for Si-H in SOG (Spin On Glass) Layer
(2) Use of ATR method to measure growth process of silicon self-oxidation

Figure 4-21 shows the results of a test in which commercial silicon (100) is etched using a dilute hydrofluoric acid and is then exposed to ambient air while the oxidation growth process is measured over time. It is evident that, along with surface oxidation, the LO mode of Si-O vibration produces a shift toward the high shift side as peak strength values rise.

Figure 4-21. Growth Process of Silicon Self-Oxidation
4.2.10 TEM (Transmission Electron Microscopy)

[Objective]
The objective of TEM (Transmission Electron Microscopy) is to permeate a thin-layer coated specimen with electrons to observe corresponding images, analyze the crystal structure, and perform elemental analysis and chemical state analysis of very small areas.

[Function]
(1) Image observation
TEM enables image observation at magnification factors of up to 10 million. Crystal defects (due to dislocation, etc.) can be observed.

(2) Crystal structure analysis
Electron beam diffraction is used to enable analysis of crystal structure, such as characteristics and crystal orientation, and to determine lattice constants.

(3) Analysis of very small areas
An EDS spectrometer and/or an EELS can also be used to enable elemental analysis and chemical state analysis of very small areas.

[Principle]
The principle of TEM is similar to the principle for optical microscopy, except that highly accelerated electrons are fired against the specimen instead of light. An electromagnetic lens is then used to obtain enlarged images of the specimen at magnification factors of up to 10 million. If the specimen has a crystalline structure, interference between permeating electron waves and diffracted electron waves can be used to obtain lattice images. Electron diffraction images can be obtained by changing the focal distance of the electromagnetic lens. These diffraction images enable analysis of the crystal structures (including crystal characteristics that distinguish among non-crystalline, polycrystalline, and crystalline structures), crystal orientation, and lattice constants in the observed area.

Elemental analysis of an area as small as 1 nm² can be performed when TEM is used with an energy dispersive X-ray spectrometer (EDS). This technology generates characteristic X-rays only from the electron beam-irradiated area while ignoring the electron beam's diffusion within the thin-film specimen, and the EDS spectrometer is then used to analyze the characteristic X-rays. The EELS (Electron Energy Loss Spectrometer), which is attached to the TEM, is used to perform elemental analysis and chemical state analysis of sites observed by the TEM. It is able to do this because of the energy loss that occurs in an electron beam as it permeates and reacts with the materials in a specimen. The energy distribution of electrons that have experienced energy loss differs in ways that reflect the local structure or atomic structure of the specimen's materials. Consequently, elemental and chemical analyses can be performed based on this energy distribution data.

When using TEM to observe semiconductor devices, a thin film must be deposited on the area that will be irradiated with an electron beam and observed. When observing silicon using a TEM set for accelerated voltage (200 kV), a film no thicker than 100 nm is appropriate. One typical film deposition method for semiconductor devices made of heterogeneous materials is a method that uses mechanical grinding and argon ions to etch the specimen. Recently, a FIB (Focused Ion Beam) device was used to deposit a thin film on an area measured with submicron precision as preparation for TEM observation. This method makes it possible to observe items such as particular wiring connection holes or particular memory cells.
TEM technology enables observation at the atomic level. TEM devices have been successfully used to evaluate interfaces between differential materials when electric resistance abnormalities occur, and to observe reactions between metal and silicon materials and cross sections of defective cells. An example of an analysis performed using TEM technology is described below.

In this example, a TEM unit is used to analyze areas where electrical resistance has increased between silicon substrates and polysilicon electrodes. By setting the magnification factor high enough to observe the crystal lattice in the silicon substrate, researchers discovered that a non-crystalline area about 1 nm thick had formed in the interface between the silicon substrate and the polysilicon (see Photo 4-8). Also, part (1) of Figure 4-23 shows an EDX profile that was taken while an electron beam was being fired specifically at that area. The EDX profile that was made from the silicon substrate for comparison purposes is shown in part (2) of Figure 4-23. These profiles indicate that oxygen, arsenic, phosphorus, and other elements are abundantly present in the silicon substrate. Armed with these analytical results, researchers were able to reduce the electrical resistance by making modifications to the preprocessing that is performed prior to growing the polysilicon.

Figure 4-22 shows an outline of a TEM system and Photo 4-8 and Figure 4-23 illustrate the above analysis example.

**Figure 4-22. Outline of TEM System**
Photo 4-8. TEM Observation Example

Figure 4-23. EDX Profile

EDX Analysis Results

Non-crystalline layer

Polysilicon

Silicon substrate

3nm
4.3 Processing Technology for Analysis

4.3.1 General
Failure analysis has become more difficult than ever due to the recent trends toward ICs that are smaller, faster, more highly integrated, and are designed using a multilayer interconnect structure. Sophistication of the processing technology is explained below.

- Faster –
  Low-resistance metal deposition techniques are increasingly required for faster ICs that need repairs, such as in wiring bypass formation or wiring connections.

- Higher integration –
  Higher integration has created the need for implementation of bypasses to enable signal input/output directly to the circuit being observed.

- Multilayer interconnect structure –
  For the analysis of a device with a multilayer interconnect structure, technique must be found to expose semiconductor elements that are formed on buried wiring layers or substrates.

4.3.2 FIB (Focused Ion Beam)

[Objective]
FIB methods are used for ultra-fine processing or image observations in which a gallium ion beam focused to a minimum width of approximately 5 nm is radiated upon the specimen. Figure 4-24 shows an outline of an FIB system.

[Function] (See Figure 4-25)
(1) Selective etching
  Etching can be performed at any site on the specimen. The site specification is accurate to within approximately 0.1 μm.
(2) Selective metallization
  When the gallium ion beam is shone upon the specimen, W(CO)₆ gas is blown onto the specimen, which is used to a tungsten layer at any specified site.
(3) Selective attachment of dielectric layer
  When the gallium ion beam is shone upon the specimen, TEOS gas is blown onto the specimen, which is used to a dielectric layer of silicon dioxide at any specified site.
(4) SIM function
  Gallium ions are fired on the specimen being scanned. The secondary electrons produced by this action are detected and their relative strength values are used to detect a contrast-based image.
[Example of analysis]

(1) Selective sectioning and observation
When using selective etching with a SIM (Scanning Ion Microscope) function, it becomes possible to slice off and observe an IC cross section at any specified site. During a three-dimensional analysis, the IC's shape can be observed as a cross section that is sliced off depthwise. This method has greatly advanced the capabilities of cross section observations. (See Figure 4-26 and Photo 4-9.)

(2) Observation of metal wiring's detailed structure
When a SIM function is used, it becomes possible to obtain images that reflect the detailed structure of metal wiring, which is to say the shape, size, and orientation of the crystal grains. This is because the mass of secondary electrons differs depending on the orientation of the crystal grains (see Photo 4-10).

(3) Selective metalization and attachment of dielectric layer
By combining selective attachment of a dielectric layer and selective metalization, it is possible to pull electrode out from metal wiring under a dielectric layer and through a metal wiring layer contained in an intermediate layer and form any desired wiring pattern or probing pad. (See Photo 4-11.)

Figure 4-24. Outline of FIB System
Figure 4-25. Four Functions of FIB

- Sputter etching
- Selective etching to small area
- Selective metal film to small area
- Selective attachment of dielectric layer in small area
- SIM
- Secondary electron

Figure 4-26. Cross-Sectioning Method Using FIB

(1) Before etching
(2) After rough etching
(3) After fine etching
Photo 4-9. Example of Cross Section Analysis

(1) Appearance of cross section

Enlargement (SIM image) of cross section

(2) Specimen with pinhole defect (shorted between first and second layer)

SIM image of cross section

Photo 4-10. Example of Extracted Electrode (When Using Selective Attachment of Dielectric Layer Function)
4. 3. 3 Sublimation processing laser

[Objective]
Irradiating the device with sublimation processing lasers (such as eximer lasers and UV lasers) removes wires or passivation layers locally and instantaneously. Irradiation is an effective processing method for analyzing layers beneath the top wiring layer, especially in the case of ICs in which wires are multilayered (Figure 4-27).

[Function]
Peeling with sublimation processing lasers can be performed concurrently with the observation of optical images via a metallographic microscope; therefore even novices can perform this easily (Photos 4-12 to 4-14).

1) Processing of passivation layers and films between layers
Any blocks can precisely be peeled or processed. Such lasers are applied to creating windows for observing waveforms, such as for wafer probing tests.

2) Processing of wiring
Removing or isolating part of wiring enables analysis of the removed or isolated areas and local function blocks. Such lasers are particularly effective in cutting thick and wide wires such as those used as power supply and ground lines.

3) Marking
When secondary electron images are used for analysis, such as when using an EB tester or FIB system, marking the chip surface beforehand (i.e., etching the protective layer) makes it easier to find the site to be analyzed.

4) Other
An excimer laser also has many other uses, such as coarse cutting before using an FIB for cross-sectioning, removing remnants after mold etching, preparing specimens before wet etching or breaking bonding wire.
[Principle]

The following describes excimer lasers, which are a type of sublimation processing lasers. An excimer laser is a type of gas laser that typically uses a mixture of rare gas and halogen gas and that fires short pulses of ultra-violet laser from a discharger. Since an excimer laser that has a short oscillation frequency has a large amount of photon energy, it is able to dissect combined molecules. The high absorptivity of the specimen's surface enables peeling processing to peel away very thin layers. The type of excimer laser that is most often used for such operations is the KrF excimer laser (wavelength: 248 nm).

![Figure 4-27. Use of Excimer Laser for Peeling Processing](image)

**Photo 4-12. Use of Excimer Laser to Cut Lower-Layer Wiring**

**Photo 4-13. Use of Excimer Laser to Expose Lower-Layer Wiring**
Photo 4-14. Use of EB Tester to Obtain Potential Contrast Image of Observed Lower-Layer Wiring

(a) Input signal: High  
(b) Input signal: Low

Reference
4.3.4 RIE (Reactive Ion Etching)

[Objective]
The objective is to expose an entire metal layer in a chip having a multilayer interconnect structure without destroying any electrical circuits or failure state.

[Function]
RIE exposes an entire metal layer in a chip without destroying any electrical circuit while removing dielectric layers (silicon dioxide, silicon nitride, silicon oxide and nitride, polyimide, etc.). The ions perform anisotropic etching, which leaves any dielectric layer below the target metal layer intact while removing all other dielectric layers. Once the entire metal layer is exposed, an EB tester or other device can be used to more effectively analyze the chip.

[Principle]
When the RIE system’s etching gas is in a plasma state, the reactive ions are accelerated by the potential gradient generating at the cathode side and the ions collide perpendicular to the chip substrate to etch the target layer.

The etching mechanism is bombarding the reactive ions onto the target layer by electrode acceleration. The target layer is activated and chemically reacts with the target layer and then the layer is changed into a volatile substance. (See Photo 4-15.)

The following techniques can be used to make anisotropic etching more effective.

1. Make a steeper sheath potential (the potential gradient that occurs at the cathode side).
2. Change the etching gas mixture (use CF₄/O₂ gas).
3. Prevent side etching (use side protection effect).
4. Prevent RIE processing of glass (change ratio of ions to radicals and use 1, 3, 5 effects).
5. Protect non-target areas (use Teflon coating).

Photo 4-15. Surface before/after RIE Processing

(1) Before RIE Processing   (2) After RIE Processing
**Photo 4-16. Cross section before/after RIE Processing**

(1) Before RIE processing

(2) After RIE processing

Etching of top wiring (metal layer with high melting point) by RIE processing (see Photo 4-16)

**References**

- M. Sanada, T. Numajiri, S. Suzuki, T. Omata “Current Abnormalities in LSIs Observed when Using RIE for Anisotropic Etching,” 1995 Spring JSAP (The Japan Society of Applied Physics) annual meeting (42nd) (Japanese version only)
4.4 List of Failure Analysis Devices

4.4.1 Devices used for visual inspection and operation analysis

Table 4-1. Overview of Devices Used for Analysis and Processing

1) Devices used for analysis

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Full Name</th>
<th>Detected Signal</th>
<th>Principle or Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>EBIC</td>
<td>Electron Beam Induced Current</td>
<td>Excitation current</td>
<td></td>
</tr>
<tr>
<td>EBT</td>
<td>Electron Beam Tester</td>
<td>Secondary electron</td>
<td>Shape observation, observation, EBIC</td>
</tr>
<tr>
<td>EMMI</td>
<td>Emission Microscope</td>
<td>Photon</td>
<td>Detection of abnormal occurring portion</td>
</tr>
<tr>
<td>LC</td>
<td>Liquid Crystal Method</td>
<td>Phase dislocation of liquid crystal</td>
<td>Detection of hot spots by optical characteristics of liquid crystal</td>
</tr>
<tr>
<td>OBIC</td>
<td>Optical Beam Induced Current</td>
<td>Excitation current</td>
<td>Junction failures or other failure sites</td>
</tr>
<tr>
<td>OBiRCH</td>
<td>Optical Beam Induced Current</td>
<td>Current change</td>
<td>Wiring resistance changes by laser irradiation is detected to the change of current</td>
</tr>
</tbody>
</table>

2) Devices used for processing

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Full Name</th>
<th>Energy Source</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>−</td>
<td>Laser</td>
<td>Removes dielectric layer</td>
</tr>
<tr>
<td>FIB</td>
<td>Focused Ion Beam</td>
<td>Secondary electrons</td>
<td>Wire cutting, hole opening in dielectric, direct etching of metal</td>
</tr>
<tr>
<td>FLB</td>
<td>Focused Laser Beam</td>
<td>Laser</td>
<td>Wire cutting, hole opening in dielectric, direct etching of metal</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive Ion Etching</td>
<td>Ions</td>
<td>Removes dielectric layer</td>
</tr>
</tbody>
</table>
4.4.2 Devices used for analytical research

Table 4-2 presents an overview of devices used for failure analysis. These devices include structure observation devices (including ordinary analytical devices) that are often used for failure analysis, and composition/status analytical devices. The type of device to be used for an actual failure analysis should be determined based on factors such as the required resolution and detection sensitivity. In such cases, the final analysis may use a combination of results from several analytical devices.

Table 4-2. Overview of Devices Used for Analytical Research (1/2)

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Full Name</th>
<th>Excitation Source</th>
<th>Signal Source</th>
<th>Principle or Method</th>
<th>Yield Data</th>
<th>Applications (Related to Electronic Devices)</th>
<th>Features (Resolution, etc.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AES</td>
<td>Auger Electron Spectrometer</td>
<td>Electrons</td>
<td>Auger electrons</td>
<td>Energy spectra of Auger electrons</td>
<td>Elemental analysis of top surface, deeper analysis is possible when ion etching is used (insulated elements are affected by electrical charge)</td>
<td>Analysis of surface contamination and surface oxidation, analysis of concentration in depth direction</td>
<td>(Minimum beam diameter) approximately 20 nm (Detection depth) up to 5 nm (Sensitivity) 0.1 to 1 A.C.% (atomic percent concentration)</td>
</tr>
<tr>
<td>EDX</td>
<td>Energy Dispersive X-ray Spectrometer</td>
<td>Electrons</td>
<td>Characteristic X-rays</td>
<td>Characteristic X-rays on an IC irradiated by an electron beam are detected by a semiconductor detector and their energy values are analyzed to identify elements.</td>
<td>Elemental analysis through study of characteristic X-rays’ energy distribution</td>
<td>Can be used with SEM and TEM devices to analyze chemical composition of very small areas.</td>
<td>(Minimum beam diameter) approximately 1 nm (when using TEM) (Sensitivity) 0.1 to 1 A.C.%</td>
</tr>
<tr>
<td>EPMA</td>
<td>Electron Probe Micro Analyzer</td>
<td>Electrons</td>
<td>Characteristic X-rays</td>
<td>Elemental analysis through detection of characteristic X-rays and non-destructive analysis. Also known as XMA (X-ray Micro Analyzer).</td>
<td>Enables observation of SEM images for chemical composition analysis</td>
<td>Analysis of surface contamination, analysis of attached impurities, analysis of film composition</td>
<td>(Minimum beam diameter) approximately 4 nm</td>
</tr>
<tr>
<td>ESCA</td>
<td>Electron Spectrometer for Chemical Analysis</td>
<td>X-rays</td>
<td>Photoelectrons</td>
<td>Measures dynamic energy of photoelectrons with weak X-ray excitation. Also known as XPS (X-ray Photoelectron Spectroscopy).</td>
<td>Used for analysis of surface elements and topology, can be used with ion etching or angle analysis as part of angle analysis.</td>
<td>Analysis of surface contamination and surface oxidation, analysis of concentration in depth direction, analysis of adhesion on metal or semiconductor surfaces</td>
<td>(Minimum beam diameter) 5 to 10 μm (Detection depth) several nm (Sensitivity) 0.1 to 1 A.C.%</td>
</tr>
</tbody>
</table>
### Table 4-2. Overview of Devices Used for Analytical Research (2/2)

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Full Name</th>
<th>Excitation Source</th>
<th>Signal Source</th>
<th>Principle or Method</th>
<th>Yield Data</th>
<th>Applications (Related to Electronic Devices)</th>
<th>Features (Resolution, etc.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FT-IR</td>
<td>FT-IR Transform Infrared Spectrometer</td>
<td>Light (infrared beam)</td>
<td>Light (infrared beam)</td>
<td>Measures spectrum of infrared beam absorption due to Fourier transforms, used with optical microscope to measure very small areas</td>
<td>Identification of substances, analysis of molecular structures, detection of impurities in trace amounts.</td>
<td>Measurement of oxidation and carbon concentration in silicon, identification of substances attached to wafer</td>
<td>Frequency &gt; 0.01 cm⁻¹</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
<td>Electrons</td>
<td>Secondary electrons and reflected electrons</td>
<td>Scans using narrow electron beam to record secondary electron strengths and reflected electrons in sync with primary electrons</td>
<td>Surface topology and composition (using EDX, etc.), surface potential</td>
<td>Analysis of materials, device surface topology, surface size, surface contamination, and impurities attached to surface</td>
<td>(Minimum beam diameter) approximately 1 nm</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectrometer</td>
<td>Ions</td>
<td>Ions</td>
<td>Detects ions that are discharged from the surface of a specimen that is irradiated by an ion beam</td>
<td>Surface and depth distributions of trace amounts of impurities</td>
<td>Dopant distribution</td>
<td>Analysis of contamination</td>
</tr>
<tr>
<td>SRP</td>
<td>Spreading Resistance Profiler</td>
<td>Voltage</td>
<td>Current</td>
<td>Needle’s contact resistance is used to determine the resistance rate and carrier concentration</td>
<td>Depth distribution of resistance rate and carrier concentration</td>
<td>Check for contamination in very low concentration, measurement of relative resistance between epitaxial layer and bulk</td>
<td>(Depth resolution) approximately 10 nm (Width of area under analysis) approximately 50 μm</td>
</tr>
<tr>
<td>STEM</td>
<td>Scanning Transmission Electron Microscope</td>
<td>Electrons</td>
<td>Electrons</td>
<td>Primary electrons are scanned on specimen, transient electrons are detected and used for image observation</td>
<td>Structure observation or analysis of composition or impurities (when EDX is also used)</td>
<td>Observation of device structure, analysis of defects and crystal structure, analysis of composition or impurities in very small areas</td>
<td>(Minimum beam diameter) approximately 1 nm</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscope</td>
<td>Electrons</td>
<td>Electrons</td>
<td>Observation of enlarged images or diffraction images of transient electrons</td>
<td>Observation of structures at atomic level, analysis of defects and crystal structure, analysis of composition or impurities (when EDX is also used)</td>
<td>Observation of device structure, analysis of defects and crystal structure, analysis of composition or impurities in very small areas</td>
<td>(Minimum beam diameter) approximately 1 nm</td>
</tr>
<tr>
<td>XMA</td>
<td>X-ray Microprobe Analyzer</td>
<td>Electrons</td>
<td>Characteristic X-rays</td>
<td>Same as EPMA</td>
<td>Same as EPMA</td>
<td>Same as EPMA</td>
<td>Same as EPMA</td>
</tr>
<tr>
<td>XPS</td>
<td>X-ray Photoelectron Spectroscope</td>
<td>X-rays</td>
<td>Photoelectrons</td>
<td>Same as ESCA</td>
<td>Same as ESCA</td>
<td>Same as ESCA</td>
<td>Same as ESCA</td>
</tr>
</tbody>
</table>
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CHAPTER 5 DESIGN SIMPLIFICATION AND RELIABILITY ANALYSIS METHODS

5.1 General

This chapter explains specific techniques, quality function deployment, parameter design, design for test, and FMEA to be used to design a semiconductor, taking specific examples.

5.2 Quality Function Deployment

Quality function deployment (QFD) was developed as a new product development tool that provides a means of communicating design concepts to the manufacturing line as well as a specific method for quality assurance.

Quality function deployment is a technique for the detailed deployment of job functions and operations to create quality, using a series of purposes and means. This technique produces favorable results by aiming to “establish design quality”, “reduce early quality problems”, “establish planned quality”, “communicate design concepts to manufacturing”, “compare and analyze our products and competitors’ products”, “help develop distinctive new products”, “clarify management issues in the manufacturing processes”, “disseminate quality information throughout the company”, “help collect and analyze market quality information”, and “reduce design changes”, and so on.

By using this technique, technologies to realize the designed quality can be developed and problems that can be foreseen can be solved systematically. This is a total quality deployment technique if it includes cost deployment that takes into consideration the price and required quality of competitors’ products, and solves bottlenecks for calculated component cost, and reliability deployment that combines a reliability technique such as FMEA to prevent failures at the design stage.

At this point, let us turn to the topic of quality tables, which play an important role in quality deployment. What are quality tables and how are they created? Quality chart is a systematic representation of terms used to describe quality-related features desired by customers. The chart shows correlation between these terms and product quality characteristics to aid the process of converting customer requirements into alternative characteristics to be used when designing products.

1) Collection of raw data
Raw data is information (requirements in plain language) received from customers with regard to particular products. This is the starting point of quality function deployment.

2) Translation to required quality
The raw data is organized into a list of required quality items. A more concise listing of quality-related terms is extracted from the raw data list, and this concise list comprises the “required quality.”

3) Creation of required quality deployment chart
Required quality items are broken down into a multileveled chart that may include primary, secondary, and tertiary levels.

4) Extraction of quality elements
Required quality items must be translated into technical terms in order to deploy customers’ abstract ideas about product quality as specific product quality characteristics. These quality characteristics are alternative characteristics that are used in place of the actual customer requirements as characteristics which can be measured and evaluated according to their quality elements (quality elements are the criteria used to evaluate quality). Usually, quality elements are extracted from the required quality items.
(5) **Creation of quality element deployment chart**

Next, quality elements are broken down into a multileveled chart that may include primary, secondary, and tertiary levels. The lowest-level items in the quality element deployment chart should be quality characteristics.

(6) **Creation of quality chart**

The required quality deployment chart and the quality element deployment chart are combined in a two-dimensional table having a matrix format. The relative strength or weakness of the correlation between required quality items and quality elements are noted using symbols (◎, ○, △, etc.). This enables importance rankings to be assigned to the required quality items and quality elements, which helps determine which quality elements are the most important.

Figure 5-1 shows an overall outline of quality deployment and Table 5-1 shows an example of a filled-in quality chart.
**Figure 5-1. Overall Outline of Quality Deployment (“House of Quality”)**

**I. Quality deployment**

- Quality characteristics
- Importance
- Comparisons with competitors
- Design quality
- Weighted quality characteristics

**II. Technical deployment**

- Comparisons with competitors
- Design quality
- Weighted quality characteristics

**1. Required quality**

- 1–I
- 1–II

**2. Weighted functions**

- 2–I
- 2–II

**3. Unit parts**

- 3–I
- 3–II

**Manufacturing method deployment**

- Process planning chart (equipment deployment)
- QC process planning chart

**Deployment to suppliers and cooperating companies**
CHAPTER 5 DESIGN SIMPLIFICATION AND RELIABILITY ANALYSIS METHODS

III. Cost deployment

<table>
<thead>
<tr>
<th>This division</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Market prices</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sales volume</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Share</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Profit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Target price</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IV. Reliability deployment

FT chart

1—IV

Required quality

2—IV

Functional deployment

2—III

2—IV

Functional deployment

Parts cost deployment

Estimated costs

Target

Weight

Cost

Bottleneck parts

NE registration No.

Switch to plastic materials

Integrated with main unit

Target Design Measures

Feedback to upstream sites

QC process charts for assembly processes

QC process charts for manufacturing processes

Work standards

Causal analysis of problems

Feedback to upstream sites
Table 5-1. Example of Filled-in Quality Chart

<table>
<thead>
<tr>
<th>Required Quality</th>
<th>Quality Characteristics</th>
<th>Primary</th>
<th>Secondary</th>
<th>Electrical Performance</th>
<th>Mechanical Performance</th>
<th>Operability</th>
<th>Designability</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Primary Importance</td>
<td>Second</td>
<td>TRS ch.</td>
<td>R characteristics</td>
<td>T characteristics</td>
<td>S characteristics</td>
<td>Durability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>C</td>
<td>B</td>
<td>C</td>
<td>A</td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>No operation errors</td>
<td>B</td>
<td>△</td>
<td>○</td>
<td>○</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Superior performance</td>
<td>A</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stable performance</td>
<td>A</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Break-resistant</td>
<td>B</td>
<td>△</td>
<td>△</td>
<td>△</td>
<td>○</td>
<td>○</td>
<td></td>
</tr>
<tr>
<td>Accident-proof</td>
<td>C</td>
<td>○</td>
<td>○</td>
<td>△</td>
<td>○</td>
<td>○</td>
<td></td>
</tr>
<tr>
<td>Easy to operate</td>
<td>C</td>
<td>△</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Easy to maintain</td>
<td>C</td>
<td>△</td>
<td>○</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Easy to replace</td>
<td>C</td>
<td>△</td>
<td>△</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Easy to attach</td>
<td>C</td>
<td></td>
<td></td>
<td>○</td>
<td>○</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attractive appearance</td>
<td>C</td>
<td></td>
<td></td>
<td>○</td>
<td>○</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good color scheme</td>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

References
- Y. Akao "Introduction to Quality Deployment" JUSE (Japanese version only)
- T. Ooffuji, M. Ono and Y. Akao "Quality Deployment Methods (1)" JUSE (Japanese version only)
5.3 Parameter Design

5.3.1 What can parameter design accomplish?

At Compound Semiconductor Devices Division, design of semiconductor products is performed based on development specifications that clearly reflect the needs of customers. At the circuit design stage, designers seek to establish a robust design that takes into account variation among manufacturing processes (a robust circuit design is a design that will not enable the circuit characteristics to be seriously affected by variation among manufacturing processes). It is also at the manufacturing design stage where variation in product dimensions, thicknesses, etc., are reduced to minimize manufacturing process variation and optimize the various manufacturing conditions and the process flow.

Thus, when circuit design, layout design, process design, device structure design, and various other aspects of design have been optimized, the result will be the building in of higher reliability.

This brings us to a definition of parameter design as design methods that minimize variation among the circuit characteristics and characteristics (parameters) that are used in manufacturing processes. The purpose of parameter design is to minimize variation among a system's output characteristics.

Generally, a large number of parameters must be established in the target system (whether it be a semiconductor device, manufacturing process, production equipment, etc.). Although a tremendous amount of tests and simulations must be performed to determine the optimum value for each parameter, parameter design offers testing and planning methods that set values for most parameters with only a minimal number of tests or simulations. The system input/output characteristics that are used in parameter design are shown in Figure 5-2.

**Figure 5-2. System's Input and Output Characteristics**

![Diagram of System's Input and Output Characteristics]

- **Input parameter X**
- **Circuit constants**
- **Variation (Δx) in manufacturing parameters, etc.**
- **System (Circuit, process, etc.)**
- **Output characteristic Y**
- **Electrical characteristics**
- **Minimize variation (Δy) in dimensions, etc. as much as possible**
5.3.2 What is parameter design?

Parameter design is one of the chief methods proposed by Gen’ichi Taguchi in his book Quality Engineering. Parameter design applies to effectively optimize the numerous parameters and thus minimizes variation in the target system's output characteristics.

Four types of S-N (signal-to-noise) ratios are defined for a system's output characteristics. These four S-N ratios are used as objective functions to optimize parameters.

SN ratio

In the context of parameter design, the SN ratio is based on regarding the variable factors in output characteristic data as “noise” and the fixed factors as “signal”. This concept of a signal-to-noise ratio is widely used in the telecommunications field, and in this case it is being extended to the field of statistical QC.

Given \( n \) as the quantity of output characteristic data:

\[ y_1, y_2, \ldots, y_n \]

Various statistical analyses are performed based on two statistical processes that use this \( n \) value:

- **Average value**
  \[ \bar{y} = \frac{\sum_{i=1}^{n} y_i}{n} \]

- **Standard deviation**
  \[ \sigma = \sqrt{\frac{\sum_{i=1}^{n} (y_i^2 - n\bar{y})}{n-1}} \]

The four types of SN ratios are defined according to the following four types of output characteristics. The input parameters are set so as to maximize the output characteristics.
(1) **Nominal-the-better characteristics**

This is the SN ratio among values centered on desired dimensions, thickness, etc.

\[
\eta = 10 \cdot \log \left( \frac{\bar{y}}{\sigma} \right)^2
\]

As shown in Figure 5-3, higher values on this curve result in lower variation \(\sigma\) among output characteristics.
(2) Smaller-the-better characteristics
This S-N ratio applies to the desire for products free of damage or defects.

Figure 5-4. Smaller-the-Better Characteristics Curve

\[
\eta = -10 \cdot \log \left( \frac{\sum_{i=1}^{n} y_i^2}{n} \right)
\]

In Figure 5-4, the SN ratio increases (improves) as the total amount (sum of amount squared) decreases.
(3) Larger-the-better characteristics

This SN ratio improves as durability and strength characteristics increase.

\[ \eta = -10 \cdot \log \left( \sum_{i=1}^{n} \frac{1}{y_i^2} \right) / n \]

Figure 5-5. Larger-the-Better Characteristics Curve

In Figure 5-5, the SN ratio increases (improves) as the total amount (sum of amount squared) increases.
(4) **Dynamic characteristics**

This SN ratio applies to the required linearity, such as in the relation between mask pattern dimensions and the finished dimensions when manufactured on a wafer.

**Figure 5-6. Dynamic Characteristics Curve**

Although no formula is given to define this SN ratio, the optimum SN ratio in this case is when the values representing correlation between inputs and outputs are as close as possible to the median straight line (see **Figure 5-6**).
5.3.3 Example of parameter design

The following is an example of how parameter design is used as part of manufacturing process design. In device manufacturing processes, the processing of electrode wiring has a major impact on yield and reliability. The conditions for the PR and dry etching processes are especially important for the stable formation of refined wiring patterns.

The following are examples of improvements made for aluminum residues in the aluminum dry etching process. As shown in Table 5-2, eight parameters (A to H) must be established for aluminum etching processes in order to consider conditions which affect the three etching sequences, such as the presence or absence of preprocessing, four types of gas flow rates, pressure, and the bias voltage.

<table>
<thead>
<tr>
<th>Etching Sequence</th>
<th>1st</th>
<th>2nd</th>
<th>3rd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flow rate of gas 1</td>
<td>known</td>
<td>known</td>
<td>known</td>
</tr>
<tr>
<td>Flow rate of gas 2</td>
<td>known</td>
<td>known</td>
<td>G</td>
</tr>
<tr>
<td>Flow rate of gas 3</td>
<td>A</td>
<td>known</td>
<td>F</td>
</tr>
<tr>
<td>Flow rate of gas 4</td>
<td>B</td>
<td>known</td>
<td>known</td>
</tr>
<tr>
<td>Pressure</td>
<td>known</td>
<td>E</td>
<td>D</td>
</tr>
<tr>
<td>Bias voltage</td>
<td>known</td>
<td>known</td>
<td>C</td>
</tr>
</tbody>
</table>

Preprocessing | H |

The orthogonal array L18 can be used to efficiently conduct a total of 18 experiments to determine the parameters to be established as parameters A to H (see Table 5-3). The three number values (1 to 3) that appear in this orthogonal array indicate the level numbers of the various factors. An S-N ratio for desired characteristics is used for aluminum residues, which have a level of zero similar to dirt and defects.
Table 5-3. Orthogonal Array L18

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;1&gt;</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<td>&lt;2&gt;</td>
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<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4.77</td>
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<td>3</td>
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<td>2</td>
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<td>1</td>
<td>2</td>
<td>3.98</td>
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<td>1</td>
<td>3</td>
<td>2</td>
<td>-9.58</td>
</tr>
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<td>1</td>
<td>3</td>
<td>-7.27</td>
</tr>
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<td>2</td>
<td>3</td>
<td>1</td>
<td>2</td>
<td>3</td>
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<td>3</td>
<td>1</td>
<td>-7.27</td>
</tr>
</tbody>
</table>

The following type of graph can be obtained by analyzing this data. (See Figure 5-7.)

The optimum conditions for the aluminum etching processes can be determined by setting factor levels that maximize the S-N ratio indicated on the Factor Effect Graph.

In this example, four factors (E, C, H, and G) are shown to have the greatest impact on aluminum residues, and we can see that the optimal conditions in this case are E = level 3, C = level 1, G = level 3, and H = level 2.

As a result of optimizing the fabrication conditions for aluminum etching processes, the occurrence of aluminum residues can be reduced while increasing both yield and reliability.

The scope of parameter design includes not only the optimization of fabrication conditions described above but also circuit design, bias design, and other areas in which it also contributes to raising the reliability and quality of ICs.
CHAPTER 5  DESIGN SIMPLIFICATION AND RELIABILITY ANALYSIS METHODS

Figure 5-7. Factor Effect Graph

References
- G. Taguchi "Quality Engineering Course 1: Quality Engineering at Development and Design Stages," (Japanese version only)
5.4 DFT (Design For Test)

The DFT (Design For Test) approach is described below as it relates to quality assurance for ICs. The higher integration of ICs has made it more difficult to comprehensively test internal circuits. Therefore, testability must be taken into consideration beginning at the design stage.

5.4.1 Testability

Testability is a characteristic that indicates the relative ease or difficulty of internal testing of circuits. Basically, testability refers to the following two qualities.

(1) Controllability
Controllability indicates the ease of setting values for internal circuits.

(2) Observability
Observability indicates the ease of observing values in internal circuits.

Several variations of these methods have been proposed as quantification methods, but these methods are the most often used for expressing separate values of combination circuits and sequential circuits by setting separate indices corresponding to “0” and “1” values.

5.4.2 Testability methods

Various methods have been developed and proposed so far as DFT methods. The following are some widely used methods.

(1) Ad hoc method
(2) Separation test
(3) Scan path test
(4) Idqq test

(1) Ad hoc method
This method is not a pre-formulated method but rather seeks to improve testability by adding pins or control logic as needed for the target circuit. One ad hoc method improves controllability by adding signal input pins or control gates for testing so that it becomes possible to directly establish the circuit's internal values to a certain extent. Another ad hoc method improves observability by adding test output pins to enable direct observation of signals from within the target circuit.

(2) Separation test
This method uses buses or other intermediate devices to enable direct input and output corresponding to specific functions. Generally, all of the input and output pins for a particular function are connected via a bus and a select signal is used to specify the function to be tested. The specified internal function can be directly tested independently from other internal circuits.
(3) Scan path
Scan path testing uses flip-flops as shift registers rather than as ordinary logic so that values can be set to the target circuit's internal flip-flops directly via test input pins without affecting the circuit's internal logic and flip-flop values can be directly observed from test output pins.
Although there are various ways to perform scan path tests, the basic theme among all scan path test methods is that control signals, clock signals, etc. are used to switch the target circuit between normal operation mode and scan path mode in which shift operations are performed to enable setting and observation of values.
The “full scan” method uses all of the target circuit's flip-flops as scan path flip-flops and the “partial scan” method uses only some of the flip-flops in this way. One advantage of the full scan method is that test patterns can be automatically generated. When using the partial scan method, note with caution that the test patterns which are obtained do not always have an adequate failure detection rate.

(4) Iddq tests
Iddq tests are techniques that are basically used for CMOS ICs. Iddq tests take advantage of the fact that, when a normal CMOS IC is in a steady state (a state in which its values do not change) it has only a very small through current, but when a defect occurs the circuits in the defective area become activated and have a large through current, which can be detected by tests that measure the supply current. Recently, Iddq tests have been increasingly used as a way to boost the failure detection rate. Since Iddq testing involves relatively little overhead (elements added for testing, etc.) it has gained attention as an inexpensive test method.
5.4.3 Application of DFT methods

As mentioned above, there are various DFT methods. From the viewpoint of obtaining adequate fault coverage and reducing overhead costs of the circuit area (gate counts), and so on, the optimum method should be selected. As a general example, general circuit testing methods such as scan path tests are used to test random logic blocks that differ according to the design. For devices such as analog multi-function ICs, separation tests and ad hoc methods are used. In addition, Iddq tests are generally used to improve overall fault coverage for CMOS circuits.

5.4.4 Tools for test

Currently, several types of CAD tools are being developed and used to implement the kinds of tests described above. Typical examples of tools that implement design for test methods include CAD tools for automatic configuration of circuits, ATGs (Automatic Test Generators) to generate test patterns, and fault simulation methods to measure the failure detection rates of generated test patterns. It is important to use these tools effectively since, for quality assurance purposes, high failure detection rates are required of test patterns used for mass-produced devices.

Test program auto generation tools for testers have been developed to enable logic IC test controls, including these test method controls, and settings to be made from an IC tester. The program check lists for every function, etc. is utilized for the analog IC. The test program auto generation tools and program check lists play an important role in improving quality assurance through the use of more suitable settings (such as for measurement items and measurement conditions) and in promoting the standardization of test programs.
5.5 FMEA

FMEA (Failure Mode and Effect Analysis) is a method whose purpose is to detect areas of incomplete design and manufacturing process or other latent defects.

This method consists in hypothesizing and enumerating the potential failure modes, potential failure influences, and potential cause mechanisms of each element making up a system. If a failure in a specific mode occurs, how the entire system is affected is classified and ranked by occurrence, influence, detection, and importance. In this way, the failures having the most serious influence can be found, countermeasures can be taken, and failures in this mode can be prevented.

The FMEA method is also useful for analyzing reliability problems in new products or small-lot products for which quantitative predictions of reliability are difficult.

The implementation steps for FMEA are described below.

(1) Make a list of the elements that configure the overall system.

(2) Hypothesize the failure modes that are expected to occur due to component failures.

(3) Hypothesize the effects on the sub system and overall system.

(4) Evaluate the extent of the effects.

(5) Study effective preventive measures.

FMEA worksheets are used to facilitate these implementation steps. (Table 5-4 shows an example of worksheet.)
### Table 5-4. Example of FMEA Worksheet

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Dicing</td>
<td>Separating wafer</td>
<td>Chip crack</td>
<td>Characteristics fail</td>
<td>Blade degradation</td>
<td>1 4 1 4</td>
<td>Blade wear control Appearance check</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Chipping</td>
<td>Characteristics degradation</td>
<td>Wafer adhesive is soft and chip</td>
<td>2 5 3 30</td>
<td>UV before dicing</td>
</tr>
<tr>
<td>Mounting</td>
<td>Gluing chip to lead frame</td>
<td>Chip peel-off</td>
<td>Open</td>
<td>Temperature low Load few</td>
<td>1 5 1 5</td>
<td>Periodically temperature measurement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Periodically load measurement</td>
<td></td>
<td>Periodically load measurement</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Chip crack</td>
<td>Characteristic fail</td>
<td>Pressure pin degradation</td>
<td>2 4 1 8</td>
<td>Periodically check of pin shape</td>
</tr>
<tr>
<td>Bonding</td>
<td>Connecting chip electrode to frame with Au wire</td>
<td>Peel-off at points A and E</td>
<td>Open</td>
<td>Temperature low Load few</td>
<td>1 5 1 5</td>
<td>Periodically temperature measurement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Periodically load measurement</td>
<td></td>
<td>Wire strength measurement</td>
</tr>
<tr>
<td></td>
<td>Improper bonding position</td>
<td>Short</td>
<td>Incorrect recognition</td>
<td>2 5 1 10</td>
<td>Appearance check</td>
<td></td>
</tr>
<tr>
<td>Mold sealing</td>
<td>Sealing chip with resin</td>
<td>Not replenished</td>
<td>Incorrect appearance</td>
<td>Projection time Mold temperature</td>
<td>1 4 1 4</td>
<td>Start-up check Periodically temperature</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Perioudically check</td>
<td></td>
<td>measurement Appearance check</td>
</tr>
<tr>
<td></td>
<td>Wire flow</td>
<td>Short</td>
<td>Projection time Mold temperature</td>
<td>1 5 2 10</td>
<td>Start-up check Periodically temperature</td>
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CHAPTER 6 USE OF SEMICONDUCTOR DEVICES

6.1 Introduction

To ensure the desired functions, performance, quality, reliability, and safety features in sets developed and manufactured by customers, both Compound Semiconductor Devices Division as the supplier of semiconductor devices and the customer as the user of such devices have roles to play in promoting safe and proper use of semiconductor devices.

As part of its role, Compound Semiconductor Devices Division implements design and manufacturing measures to ensure the quality, reliability, and safety of semiconductor devices, provides product labels and documents describing use-related cautions and restrictions, and recommends appropriate products for each application. The various quality assurance measures that Compound Semiconductor Devices Division implements during semiconductor device development, manufacture, and sales have been described in Chapter 1.

The measures to be implemented by customers who develop and manufacture sets include selecting semiconductor devices that have quality and reliability features that are appropriate for the set's requirements, avoiding the application of stresses that exceed the device's stress resistance capacity, implementing design for safety and other safety measures for each set, and fully implementing evaluation of each set's functions, performance, quality, reliability, and safety features before using the set.

With the above considerations as a backdrop, this chapter presents general use-related general cautions for semiconductor devices deemed necessary to ensure the quality, reliability, and safety of sets. These cautions concern the set design, handling, packaging, storage, shipment, and testing of devices as well as issues such as ESD, latchup, and device mounting.

Customers should refer to individual device documentation (manuals, etc.) for cautions pertaining to specific semiconductor devices in addition to understanding the general cautions described in this chapter.

6.1.1 Product safety

Ordinarily, semiconductor devices are not hazardous products (i.e., they do not emit toxic gas, etc.). Consequently, semiconductor safety considerations relate to safe handling of semiconductor devices in the sets being designed by customers, improving fire resistance, and minimizing the environmental impact of disposing of sets that are no longer used.

To promote the customer's safe use of semiconductor devices in sets, this chapter also provides various information concerning set design.

To help improve fire resistance under actual use conditions, Compound Semiconductor Devices Division has made sure that all of its plastic-encapsulated semiconductor products use plastic materials that meet UL standards for flame resistance. Specifically, depending on the product, it may be the product itself that has received UL certification or only the plastic material used in the product.

To help minimize the environmental impact of set disposal, Compound Semiconductor Devices Division performs safety and environmental safety assessments on semiconductor devices as part of its product design assessment audits.
6.2 Cautions on Designing Sets

6.2.1 Cautions on selection of devices

(1) Application-related cautions

The first requirement for using semiconductor devices is to select a semiconductor device that is appropriate for its intended use: in other words, it must have the quality and reliability features needed for the target electronic equipment. At NEC Electronics Corporation Compound Semiconductor Devices Division, semiconductor device applications are divided into the three categories of standard applications, special applications, and specific applications according to the amount of risk associated with the target electronic equipment in terms of human life, property, social factors, and environmental factors (see Table 6-1).

Table 6-1. Application Categories for Semiconductor Devices

<table>
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<tr>
<th>Application Category</th>
<th>Examples of Electronic Equipment</th>
<th>Applicability of Standard Products</th>
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<tr>
<td>Standard applications</td>
<td>Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, household electronic appliances, personal electronic equipment, machine tools, industrial robots, etc.</td>
<td>Applicable</td>
</tr>
<tr>
<td>Special applications</td>
<td>Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment, and medical equipment (not specifically designed for life support), etc.</td>
<td>Applicability depends on product</td>
</tr>
<tr>
<td>Specific applications</td>
<td>Aircraft, aerospace equipment, submersible repeaters, incineration control equipment, nuclear reactor control systems, life support systems or medical equipment for life support, etc.</td>
<td>Not applicable</td>
</tr>
</tbody>
</table>

The quality grade of semiconductor devices designed, developed, manufactured, and sold by NEC Electronics Corporation Compound Semiconductor Devices Division is NEC Electronics “Standard” unless otherwise specified in NEC Electronics Corporation Compound Semiconductor Devices Division data sheets, technical note, shipment specifications, etc. NEC Electronics standard products are intended for use in electronic equipment that falls under the category of general applications. Consequently, such products are not designed, developed, and manufactured for use in specific applications in which there is a risk of property damage, personal injury, or serious social or environmental impacts. In other words, standard-grade NEC Electronics Corporation Compound Semiconductor Devices Division products should never be used for “specific” applications such as those listed in Table 6-1.

Customers should be aware that NEC Electronics Corporation Compound Semiconductor Devices Division semiconductor products should never be used for “specific” applications (aeronautical equipment, aerospace equipment, submersible repeaters, incineration control equipment, nuclear reactor control systems, life support systems or medical equipment for life support, etc.) unless authorization has been received from the person responsible at NEC Electronics Corporation Compound Semiconductor Devices Division.

Semiconductor devices that are intended for special and/or specific applications must have appropriately high quality and reliability grades. Therefore, NEC Electronics standard grade products must be checked for applicability before being used for “special” applications, and devices having quality and reliability grades exceeding those of standard devices must be developed for “specific” applications.

The quality and reliability grades of NEC Electronics standard products differ greatly depending on the device type (discrete semiconductor, IC, etc.). Thus, some standard grade devices can be used without modification for certain “special” applications while others must additionally undergo a quality assurance program before being used for such applications.
Before using an NEC Electronics standard grade device for a “special” application, customers should be sure to make a full evaluation of the device’s applicability and must obtain written authorization from NEC Electronics Corporation Compound Semiconductor Devices Division for the target application. The authorization that is issued with the shipment specifications can be used in lieu of such written authorization.

For semiconductor devices that are used for “specific” applications, a special quality assurance program (encompassing all processes from design to manufacture and inspection) is required for such devices instead of the quality assurance program used for NEC Electronics standard grade devices. This quality assurance program must meet the quality requirements (in terms of required device quality or quality assurance programs) of customers who design and manufacture electronic equipment for “specific” applications. When NEC Electronics Corporation Compound Semiconductor Devices Division’s staff receive an order for semiconductor devices that will be used in electronic equipment for “specific” applications, they first determine whether or not NEC Electronics Corporation Compound Semiconductor Devices Division is able to provide such devices. If NEC Electronics Corporation Compound Semiconductor Devices Division is able to provide them, the order is formally received based on a quality assurance contract or agreement as well as a shipment specification.

Consequently, any customer who is considering using an NEC Electronics standard grade semiconductor product for electronic equipment that is categorized as a non-standard application (i.e., a special application, specific application, other application that requires high reliability, or an application that the customer judges as requiring quality and/or reliability exceeding that of general electronic equipment) is strongly advised to first consult with a local NEC Electronics Corporation Compound Semiconductor Devices Division sales representative.

(2) Cautions on selection of standards

(a) Maximum ratings
The maximum ratings for semiconductor devices are ordinarily specified as “Absolute Maximum Ratings”. Absolute maximum ratings are defined under JIS C 7032 as limit values that must not be exceeded even momentarily or limit values that must be simultaneously maintained for several parameters when ratings have been specified for those parameters. Absolute maximum ratings are provided for voltage, current, power, and temperature and are defined separately for individual product. When selecting a semiconductor device, be sure to check the relevant data sheet to ensure compliance with the absolute maximum ratings for the device in question.

(b) Derating considerations
Derating is defined under JIS Z 8115 as the systematic reduction of load for the sake of improved reliability. At the system design stage, some amount of derating may be necessary when taking into account factors such as surge and noise.

The derating characteristics differ depending on the device in question, but derating is generally done for electrical stress such as voltage, current, and power as well as for environmental stress such as ambient temperature and humidity.

Heat sink design requirements place certain restrictions on power devices in particular. Derating for such devices should be done with extreme caution since the amount of derating in relation to the maximum ratings can have a serious impact on reliability.
(c) Safe operating areas in transistors

When a transistor is used as a switching element in an inductive-load circuit, SOAs (Safe Operating Areas) must be considered in addition to maximum ratings.

Figure 6-1 describes SOAs in the following four types of elements.

1. **Area I**........... \( I_c \) (\( I_d \)) MAX
   
   This area is restricted by the collector (drain) current rating.

2. **Area II**........... Dissipation Limit
   
   This area is restricted by the total dissipation (thermal resistance).
   
   In the case of direct current (DC), the limit varies according to the thermal resistance \( R_{thj-c} \), and in the case of pulse, the limit varies according to the transient thermal resistance \( \Delta R_{th} \), as shown in Figure 6-2.

3. **Area III**........... Secondary breakdown limit
   
   This area is limited by secondary breakdown phenomena.
   
   Failure mechanisms that exceed this limit are described in 3.3.5 of Chapter 3 above.
   
   Figure 6-3 shows derating curves used in relation to case temperatures.

4. **Area IV**........... \( V_{CE0} \) (\( V_{DS0} \)) MAX
   
   This area is limited by the collector (drain) voltage rating.

---

**Figure 6-1. Example of Safe Operating Area**

- **Collector current \( I_c \) (A)**
- **Collector to emitter voltage \( V_{CE} \) (V)**

(Note)
1. \( T_c = 25^\circ \text{C} \)
2. Dissipation limit area should be derated according to the case temperature and duty cycle.
3. The secondary breakdown limit area corresponds to a single pulse.
   
   This area should be derated according to the case temperature.
Figure 6-2. Example of Transient Thermal Resistance Characteristics

![Transient Thermal Resistance Characteristics](image)

\[ V_{cc} = 10 \text{ V} \]
\[ I_c = 3.0 \text{ A} \]
\[ \text{Duty} = 0.001 \]

- Without heat sink
- With heat sink \((R_{th} = 2.5 \degree C/W)\)

Figure 6-3. Safe Operating Area Derating Curves

![Safe Operating Area Derating Curves](image)

(a) When \( T_{j\text{MAX.}} = 150\degree C \)
(b) When \( T_{j\text{MAX.}} = 175\degree C \)

(Note) When \( T_c > 25\degree C \), this derating factor is applied to the safe operating area's current value.
(3) Package selection
Semiconductor device package types include two main types: (1) hermetic sealed packages, such as metal sealed packages, ceramic sealed packages, glass sealed packages, low melting point glass sealed CERDIP (CERamic Dual-Inline Package) packages; and (2) plastic encapsulated packages.
In addition, packages are categorized as either THD (Through Hole Device) packages or SMD (Surface Mounted Device) packages according to how they are mounted.
Recently, progress in high-performance, downsized, and low-cost application sets that use semiconductor devices has led to the development of highly integrated ICs. Accordingly, ICs are equipped with more pins and made thinner, transistors are also miniaturized and made thinner, and a larger choice of structures and mounting methods has become available.
The semiconductor device package (characterized by encapsulation type, shape, leads, etc.) that is used in a customer set (equipment or systems) should be selected from among the various available packages as the package that best meets the set's entire array of requirements including its use objective, size, shape, use environment, reliability targets, device mounting conditions, and so on.
When designing such sets, package-oriented device selection should be based on how well the package's shape, functions, performance features, and reliability features meet the above-mentioned set requirements.
For the specific package type and standard, refer to the product information on Compound Semiconductor Devices Division web site.
URL http://www.ncsd.necel.com/

6.2.2 Cautions concerning design for safety

(1) What is design for safety?
In the EC Mechanical Directives and U.S. MIL standards (MIL-STD-882), the following principles are set forth concerning the following type of design for safety efforts with regard to products, equipment, and systems.
<1> Design to minimize risks. (Design for Safety Principle 1)
<2> Use safety devices and/or protective measures to reduce any risks that cannot be eliminated. (Design for Safety Principle 2)
<3> If an unacceptable amount of risk still exists after safety devices and/or protective measures are introduced, attach warning labels concerning the risk. (Design for Safety Principle 3)
<4> Establish clear-cut training procedures for users concerning all work processes including proper wear of protective garments. (Design for Safety Principle 4)

Here, the term “risk” means the probability and extent of damage or injury that can result from a product or equipment unit. The extent of damage or injury is measured by the degree of damage or injury to human life, property, or the environment.
Under current product liability laws, the existence of defects in manufactured goods is a correlation between the utility of the manufactured goods (products, equipment, etc.) and the amount of risk as defined above, and such defects are judged to exist when a risk exists that is not within the design tolerances or socially accepted norms. If damage or injury to human life, property, or the environment occurs due to a manufactured product and if the existence of a defect in said product is confirmed, it is common knowledge that the manufacturer bears liability for compensation of the damage and/or injury.
Design for safety as it relates to products and equipment is intended to prevent damage or injury to human life, property, and the environment by eliminating or at least reducing to acceptable levels any risk of such damage or injury. Therefore, the types of design measures described in <1> to <4> above are implemented as part of the design for safety approach.
Regardless of whether or not the above-mentioned EC directives or MIL standards are applied, it is clearly essential for design for safety to be implemented as part of the company’s obligations toward the customers of the client companies that plan, design, develop, and manufacture sets as well as toward society as a whole. For its part, Compound Semiconductor Devices Division implements a variety of design-, manufacturing-, and labeling-related measures to eliminate or at least minimize faults and defects in semiconductor devices. Compound Semiconductor Devices Division’s design for safety approach should be obvious based on an understanding of this manual’s contents.

In view of the above liability considerations, all of Compound Semiconductor Devices Division’s semiconductor product data sheets, technical note, and other documentation include the following message concerning product liability.

While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.

(2) System safety concepts
Most of the sets or electronic equipment units that use semiconductor devices are system products, as is typical of high-tech products. As such, these products tend to contain numerous parts, materials, components, software, and sub systems that have been manufactured or purchased by set manufacturers (Compound Semiconductor Devices Division customers), all of which are integrated according to the use objectives. Furthermore, in many cases, such system equipment is often used in combination with other system equipment models that are manufactured by a third party. Accordingly, the safety of system equipment profoundly depends on the functions and safety of the third-party system equipment as well as on the parts, materials, components, software and sub systems that comprise the system equipment.

Design for safety as it relates to such system equipment goes beyond the concept of product safety (PS) and is instead based on what MIL-STD-882 refers to as “system safety”.

The system safety concept refers to systematic engineering and management methods to optimize the safety of systems. These methods have the following two characteristics.

<1> Clearly defined management of the interface conditions existing among parts, materials, components, software, sub systems, the people using systems, and the use environment, along with clarification of the risk-related liabilities.

<2> Evaluation of risks at each phase in the life cycle of a system, from planning to design, development, manufacture, operation, and disposal, along with planning to eliminate or reduce such risks.

Compound Semiconductor Devices Division asks all of its customers to implement design for safety with regard to the sets they manufacture, based on the above system safety concept.

(3) Design for safety concerning sets that use semiconductor devices
When designing a set that uses semiconductor devices, the above-mentioned system safety concept demands that design for safety be implemented so as to evaluate the risk of failures and defects in semiconductor devices at every phase in the set’s life cycle and to eliminate such risks or reduce them to acceptable levels.

The first step in design for safety for sets that use semiconductor devices is to select semiconductor devices that have the required quality, reliability, and safety characteristics. The second step is to select the most important elements in terms of reducing applied stresses.
CHAPTER 6 USE OF SEMICONDUCTOR DEVICES

The amount of risk that is considered acceptable differs according to the application. The “specific” applications described earlier have the lowest levels of acceptable risk. Therefore, it becomes necessary to select semiconductor devices that have sufficiently high reliability ratings and/or low failure rates to keep risks within the levels required for such applications.

The reliability, degradation, and failure of semiconductor devices also depends on the amounts of various stresses that are applied to semiconductor devices, such as voltage, current, power, temperature, humidity, mechanical stresses such as vibration and shock, thermal stresses, electromagnetism, light, radioactive rays, corrosive gas, and dust.

Therefore, a set’s design conditions, use conditions, and environmental conditions shall not only meet with maximum allowable stress levels of semiconductors to be used, but shall also have stress levels set as derated as possible.

Appropriate derating of stress, along with careful selection of devices with a view toward appropriate quality, reliability, and safety features for the target set will enable risks associated with semiconductor device faults or defects to be eliminated or reduced, which in turn will eliminate or reduce to acceptable levels the risks associated with the target set that contains semiconductor devices.
6.2.3 Cautions on circuit design

(1) General cautions

It is known that CMOS IC operates abnormally or breaks down if latchup occurs (for the latchup occurrence mechanism, the withstand voltage testing method, and countermeasures to be taken during device design, see 3.2 Principal Failure Modes and Failure Mechanisms in CHAPTER 3).

For reliability designing, preventing malfunctioning or functional degradation due to noise and external stress, and safety designing, the following measures should be taken in designing a circuit.

(a) Set operating conditions such as voltage, current, power, and ambient temperature within the maximum ratings.

(b) Carefully design heat radiation and keep the ambient as low as possible.

(c) Suppress variation in the supply voltage applied to the semiconductor product to within ±10%.

(d) Isolate GND lines.

(e) Insert filters or other mechanisms to attenuate surges on power supply lines.

(f) Insert (between VDD and GND) capacitors matched to the frequency for eliminating surge or noise to each node of the PCB power supply lines.

Examples: High-frequency filter: 0.01 to 0.1 μF
Low-frequency filter: 10 to 100 μF

(g) Use a low-impedance shield line for long wiring on the PCB.

(h) Suppress the noise level by inserting (parallel to noise sources) diodes and capacitors that have good high-frequency characteristics.

(i) Set up correction circuits to increase the noise margin in target circuits.

(j) Be careful to minimize external stress factors (noise, surges, vibration, ambient temperature, environmental factors, etc.).

(k) Avoid generation of static electricity discharges during use or minimize their effect.
(2) Cautions concerning circuit design of systems using ICs

(a) Cautions related to power activation

ICs are susceptible to being damaged as a result of any overcurrent that flows during the interval between power on and reset signal input. Such an overcurrent may be floating in the IC before power on and may flow if it is not first initialized. Inputting a reset signal initializes the IC and eliminates overcurrent. ICs that have a power on reset circuit never have such overcurrent flow problems.

As shown in Figure 6-4, when the IC’s shared I/O pins are used in input mode, any external output circuit that outputs a signal should be connect to one of these pins. Right after the power is activated, the IC remains internally uninitialized, so it is impossible to know when the IC’s internal output enable signal becomes active (high). Thus, when the IC’s internal output buffer and an external output circuit have different potentials, an overcurrent measuring at least several dozen mA flows. If a reset signal is input, all shared I/O pins will be set to input mode (output enable signal becomes inactive), stopping the overcurrent’s flow.

Perform the following measures to prevent overcurrent damage at power on.

<1> Insert a resistor (about 1 kΩ) between the external output circuit and the shared I/O pin. Note, however, that in such cases the resistor may reduce the propagation speed of the output signal from the external output circuit.

<2> Set up a power on reset circuit external to the IC and input a reset signal and a power on signal at the same time.

Figure 6-4. Example of IC with Reset Signal Input Pin
(b) Cautions on load drivers

IC output circuits have a maximum output current rating. If the resistance value is too low, such as in a current limiting resistor for an LED driver (shown in Figure 6-5) or in an open drain pin's pull-up resistor (shown in Figure 6-6), the IC risks being damaged by an overcurrent. Be sure to determine resistance values that will keep the output current to within the rated values.

Figure 6-5. Caution 1 Concerning Load Driver

Figure 6-6. Caution 2 Concerning Load Driver
6.2.4 Cautions on thermal designing

(1) General
The effects of thermal factors on the reliability of semiconductor devices during actual use can be profound. In particular, the advent of ever smaller, flatter, and faster semiconductor devices in recent years has made thermal resistance a matter that cannot be ignored.

The operating junction temperature of ordinary semiconductor devices is determined by a mutual interaction between temperature conditions in the device's environment and increases in junction temperature that occur within the devices themselves. This chapter describes methods for measuring and calculating the heat propagation and thermal resistance within semiconductor devices.

Structure of semiconductor devices
Before getting fully into this topic, let us consider the structure of semiconductor devices. Figure 6-7 illustrates an SMD that has been mounted on a PCB.

Figure 6-7. Example of SMD Mounted on PCB
(2) Heat propagation
Generally, heat is propagated in three ways: by conduction, convection, and radiation. In SMDs, heat propagation is determined by conduction and convection, as shown in Figure 6-8 (the principles of conduction and convection are not explained here).
Heat that occurs at a junction is dispersed by thermal conduction to various other areas, after which it is released to the outer air by convection from the surface of the SMD. However, an adiabatic condition occurs in the gaps between the surface of an SMD and the PCB due to the fact that the gap is too narrow (less than 1 mm) to disable convection. The ease (or difficulty) with which heat is propagated is called thermal resistance.

Figure 6-8. Propagation of Heat in SMD

(3) Thermal resistance
This is a brief description of thermal resistance in semiconductor devices. Figure 6-9 shows an equivalent circuit describing thermal resistance.

Figure 6-9. Thermal Resistance in Equivalent Circuit

Thermal resistance in semiconductor devices can be categorized as follows according to the way in which heat is propagated.
- Thermal conduction: Thermal resistance from junction to case ($R_{thj-c}$)
- Convection: Thermal resistance from case to ambient air ($R_{thc-a}$)
The formula for these two types of thermal resistance is shown below.

\[(R_{thj} - a) = (R_{thj} - c) + (R_{thc} - a)\]

During actual use conditions, when a semiconductor device is mounted on a PCB, thermal conduction occurs from the mounted case to the PCB, which broadens the heat dissipation area. Accordingly, thermal resistance \((R_{thc} - a)\) can be reduced by mounting the semiconductor device.

(4) Measurement of thermal resistance

Thermal resistance measurement methods include the \(\Delta V_{BE}\) method (for bipolar transistors), the \(\Delta V_{DS}\) method (for MOS FETs), and the \(\Delta V_{GS}\) method (for GaAs FETs). The \(\Delta V_{BE}\) method is described below.

The \(\Delta V_{BE}\) method uses the temperature dependence of a transistor’s \(V_{BE}\) (ON) state to determine thermal resistance based on the variation value of \(V_{BE}\) (ON) when power is applied to the transistor being measured.

Figure 6-10 shows an equivalent circuit and the measurement timing.

During an actual measurement, the common practice is to mount the semiconductor device’s heat source and a similar transistor chip on the package to measure via simulation.
(5) Example of actual measurement

Figure 6-11 shows an example of measuring transient thermal resistance in a 20-pin QFN package.

Figure 6-11. Example of Measuring Transient Thermal Resistance of 20-Pin QFN Package
(6) Formula for calculating thermal resistance

The thermal resistance evaluation data is analyzed in relation to each factor in order to derive a thermal resistance calculation formula. This formula is shown below. Note, however, that individual measurements are required for special packages (such as packages that include a heat spreader). During actual use, these packages are greatly affected by the use environment (ambient temperature, air currents, etc.).

**<DIP and THD packages>**

\[
(R_{thj} - a) = (R_{thj} - c) + (R_{thc} - a)
\]

\[
(R_{thj} - c) = 6.15 \times 10^{-7} \frac{V_T^{0.922}}{I_f^{0.08} \times S_f^{0.15} \times a^{0.046}}
\]

\[
(R_{thc} - a) = 320 S_A^{-0.705}
\]

(However, this is when \(S_A\) is no greater than 15 cm².)

- \(R_{thj} - a\): Thermal resistance between junction and ambient air [°C/W]
- \(R_{thj} - c\): Thermal resistance between junction and case [°C/W]
- \(R_{thc} - a\): Thermal resistance between case and ambient air [°C/W]
- \(\lambda_R\): Thermal conduction rate in resin [J/cm • sec • k]
- \(S_f\): Surface area of island [cm²]
- \(V_T\): Volume of IC [cm³]
- \(a\): Area of heat source [cm²]
- \(S_A\): Surface area of IC [cm²]

**<SMD package>**

\[
(R_{thj} - a) = (R_{thj} - c) + (R_{thc} - a)
\]

\[
(R_{thj} - c) = 0.295 \frac{1}{\lambda_R^{0.512} \times \lambda_L^{0.276} \times S_L^{0.50} \times a^{0.254}}
\]

\[
(R_{thc} - a) = 260 S_A^{-0.629}
\]

\[
(R_{thc} - a) = \frac{1}{2} 260 S_A^{-0.629}
\]

(50 mm × 50 mm × 1.6 mm, all copper foil glass epoxy PCB)

- \(R_{thj} - a\): Thermal resistance between junction and ambient air [°C/W]
- \(R_{thj} - c\): Thermal resistance between junction and case [°C/W]
- \(R_{thc} - a\): Thermal resistance between case and ambient air [°C/W]
- \(\lambda_R\): Thermal conduction rate in resin [J/cm • sec • k]
- \(\lambda_L\): Thermal conduction rate in L/F [J/cm • sec • k]
- \(S_L\): Area opposite island lead [cm²]
- \(a\): Area of heat source [cm²]
- \(S_A\): Surface area of IC [cm²]
Since power packages are generally used with an attached heat sink, unlike DIP and SMD packages their thermal resistance between the junction and case (\(R_{thj - c}\)) is very significant. Figure 6-12 shows an abbreviated diagram of a T-92 package with attached heat sink that is used for power supply devices.

\begin{align*}
(R_{thj - a}) &= (R_{thj - c}) + (R_{thc - a}) \\
(R_{thj - c}) &= R_{thh(p)} + R_{thh(s)} + R_{thh(c)} \\
R_{thh(p)} &= 0.65a^{-1} \sqrt{2.47l_p^2} \\
R_{thh(s)} &= 0.33 \left(a + 2l_p\right)^{-2} \sqrt{108.5l_s^2} \\
R_{thh(c)} &= 0.125 \left(a + 2l_p + 2l_s\right)^{-3} \sqrt{5.67l_c^2} \\
(R_{thc - a}) &= 310S_h^{-0.769}
\end{align*}

(\(R_{thj - a}\)): Thermal resistance between junction and ambient air [°C/W]  
(\(R_{thj - c}\)): Thermal resistance between junction and case [°C/W]  
(\(R_{thc - a}\)): Thermal resistance between case and ambient air [°C/W]  
\(R_{thh(p)}\): Thermal resistance of chip [°C/W]  
\(R_{thh(s)}\): Thermal resistance of solder [°C/W]  
\(R_{thh(c)}\): Thermal resistance of stem [°C/W]  
\(l_p\): Chip thickness – junction thickness [cm]  
\(l_s\): Solder thickness [cm]  
\(l_c\): Stem thickness [cm]  
\(S_h\): Surface area of IC [cm²]
Supplement: Transient thermal resistance in power packages

The transient thermal resistance of a bar (length L) shown in Figure 6-13 is calculated by using the Mortenson theory as listed below (where radiation and convection are ignored).

Figure 6-13. Transient Thermal Resistance in Power Package

\[
\theta(t) = \theta_0 \left[ 1 - \frac{8}{\pi^2} \sum_{n=1,3,5,...} \frac{\exp\left( \frac{n^2\pi^2dL}{4L^2} \right)}{n^2} \right]
\]

(1)

when \( t < 0.1 \tau_1 \)

\[
\theta(t) = \theta_0 \left[ \frac{t}{2\tau_1} + \frac{L}{\lambda A} \frac{t}{2\tau_1} \right]
\]

\[
\tau_1 = \left( \frac{2L}{\pi} \right) \times \left( \frac{1}{k} \right) \quad k = \frac{\lambda}{C_p \rho}
\]

Actually, since the heat source area is usually smaller than the conductor area in the case of Tr, a 45° model is used.

The 45° model is shown in Figure 6-14.
Figure 6-14. 45° Model

Heat source (one side, a)

The saturated thermal resistance in this case is expressed as follows.
\[ \theta_b = \frac{1}{\lambda} \int_{0}^{x_1} \frac{dx}{(a + 2x)} \quad (2) \]

When this is integrated:
\[ \theta_b = \frac{1}{2\lambda} \left[ \frac{1}{a} - \frac{1}{a + 2x_1} \right] \quad (3) \]

Here, (3) is used instead of (1) to obtain the transient thermal resistance as follows.
\[ \theta(t) = \frac{1}{2\lambda} \left( \frac{1}{a} - \frac{1}{a + 2x_1} \right) \sqrt{\frac{t}{2\tau_1}} \quad (4) \]

In an actual IC, the chip, solder, and stem have a multilayer structure, so equation (4) can be used for these calculations (matches with actual test).

(7) Summary

In the recent trends toward smaller, flatter, and faster ICs, heat has become an important factor affecting reliability. At the same time, the amount by which thermal resistance can be lowered in semiconductor devices themselves is approaching the limit.

Given this situation, the thermal design of entire systems that include semiconductor devices is becoming an increasingly important issue.

Therefore, we believe it is essential that the various semiconductor manufacturers share all of their knowledge concerning thermal resistance to help spur progress in this area.
6.2.5 Cautions on use environment

This section describes cautions on the storage and use environments of semiconductor devices that are built into a set or electronic equipment unit.

(1) Temperature environment

A set (not conducting electricity) must be stored within the rated storage temperature range of semiconductor devices. The electrical characteristics of semiconductor devices are temperature-dependent and are therefore sensitive to the environmental temperature. To preserve the desired electrical characteristics, the ambient temperature or the case temperature must be kept at least within the temperature range required for guaranteed operation. However, in order to prevent degradation of semiconductor devices and prolong their service life, it is desirable to further derate the operating temperature below the maximum rated value.

When a set is in operation (conducting electricity), the temperature of the set's internal semiconductor devices rises as the ambient temperature or case temperature rises relative to the storage temperature. Taking into consideration such rises in the use environment temperature and the set's internal temperature, the design must keep these temperatures within the range that ensures the electrical characteristics and service life of the semiconductor devices.

(2) Humidity environment

The set should be designed and used in a manner that maintains humidity within the case in the range of 40 to 75% (RH) during both storage and use.

Also, avoid using a set in places where condensation may occur, such as a tightly enclosed room or a place where the temperature changes rapidly.

If a set is used for a long time in a highly humid environment or an environment in which condensation occurs, plastic-encapsulated semiconductor devices may absorb moisture since they are not air-tight, and such moisture absorption can cause chip degradation or faults. Recent semiconductor devices tend to have higher pin counts and a smaller pin pitch (interval between lead pins), which makes it easier for leakage to occur between pins on the PCB, which in turn can cause operation faults.

If a high-humidity environment cannot be avoided due to the purpose of use or the installation site, appropriate anti-humidity measures should be implemented for the semiconductor devices and the PCB.

When a set is used in a low-humidity environment, there is a risk of semiconductor device wear or damage due to electrostatic discharges (ESD). If a low-humidity environment cannot be avoided, be sure to implement ESD countermeasures such as those described in 6.4 below.

(3) Strong electromagnetic field

If a set contains a power supply that generates a strong electromagnetic field or if a strong electric field or electromagnetic field is otherwise generated near a set (such as office equipment, production machinery, etc.), the set or its internal circuits may suffer electromagnetic disturbances. Such disturbances include conduction noise on power supply lines or telephone lines or radiant noise that is propagated as electromagnetic waves. These types of disturbances cause noise to occur in semiconductor devices or circuits, which can lead to operation faults.

To prevent circuit function faults caused by electromagnetic disturbances, optimize the circuit layout pattern on the PCB, make the power supply and GND lines thicker, use shield lines, and design the layout so that electromagnetic shields are also attached to semiconductor devices or circuits.
(4) **Radioactive rays**
Semiconductor devices that are not designed to be anti-radioactive devices may suffer wear or operation faults caused by radioactive rays or strong cosmic rays. Unless otherwise noted, NEC Electronics Corporation Compound Semiconductor Devices Division’s standard-grade semiconductor devices are not designed as anti-radioactive devices. Therefore, when using such devices in an environment in which radioactive rays may be generated or received, design measures must be taken to shield the semiconductor devices or circuits from radioactive rays and cosmic rays.

(5) **Corrosive gas, salty air, dust, oil fumes, etc.**
If semiconductor devices are used in an environment containing a corrosive gas such as SO or NO or if the air is very salty, leads can become corroded, causing degradation of characteristics. If such an environment is also a high-humidity environment, such degradation can accelerate and a large amount of leakage may occur due to chemical reactions between leads.

If semiconductor devices are used in an environment containing a lot of dust or oil fumes, similar degradation or leakage between leads may occur due to the humidity-preserving tendencies of dust and oil. Therefore, use in such environments should be avoided or, if unavoidable, the set design should include measures to prevent such degradation or leakage between leads.

(6) **Vibration, shock, and stress**
Semiconductor devices should be designed, manufactured, stored, shipped, and used in ways that protect them from exposure to vibration, shock, mechanical stresses, and thermal stresses during their entire service life from PCB mounting to usage in sets.

When a strong vibration, shock, mechanical stress, or thermal stress is applied to a semiconductor device, problems such as reduced reliability, wire breakage, and package or chip cracking may occur. Special care should be taken to avoid exposing semiconductor devices to mechanical shock and thermal shock as they are mounted, as well as to vibrations or shocks that can occur during shipment or use of sets.

(7) **Optical effects**
Optoelectronic effects in semiconductors is a well known issue and irradiating a semiconductor device in light can cause electromotive force to occur, which can lead to operation faults.

To prevent leakage or operation faults that may occur due to irradiated light, design sets so that their semiconductor devices are not unnecessarily exposed to direct sunlight, ultraviolet rays, fluorescent lamps, etc.

(8) **Smoke and flames**
Since semiconductor devices are not fireproof, there is a risk that such devices may begin to smoke or burn when exposed to an overcurrent. Toxic gas may also be emitted from smoking or burning devices.

To prevent such occurrences, overcurrent prevention measures such as inserting series resistors between the power supply and semiconductor devices may be required to prevent overcurrents from flowing when an operation fault or a short occurs. Also, the set's operation manual should clearly instruct set operators to avoid using sets in the vicinity of heating elements, ignescent materials, or flammables.

(9) **External noise**
If the wiring (such as of I/O signal lines) of the PC board is too long, noise and surge influences due to external induction are likely, and some devices may malfunction.

To prevent this from happening, the wiring length must be kept short, the impedance must be lowered, and a noise eliminator must be inserted.
(10) Electromagnetic interference

Electromagnetic interference waves include conductive noise that is transmitted over power supply lines and telephone lines, and radiation noise that is directly radiated from a system as electromagnetic waves. The measurement method and countermeasures to be taken against these waves differ for each type of noise. One aspect that makes it difficult to prevent and contain these waves is that there is no way to calculate the strength of the electromagnetic waves generated from the respective parts of the system at the design stage. It is important to select and provide optimum shielding to the finished product, taking the measurement result for the finished product into consideration.
6.3 Cautions on Packing, Storage, Shipment, and Handling

Although semiconductor devices generally have high quality and high reliability, they are susceptible to damage or degradation when handled improperly. The following are cautions on the handling of packing containers as well as the packing, storage, and shipment of semiconductor devices.

6.3.1 Cautions on handling packing containers

Compound Semiconductor Devices Division uses packing containers whose materials and structure are designed to preserve the original quality of the semiconductor devices they contain, even under the worst environmental conditions. Note the following cautions when handling these packing containers (see Figure 6-15).

Figure 6-15. Packing Containers

(1) Tray containers
When using a tray container that enables semiconductor devices to be divided into small groups, be careful to avoid bending of leads that can occur when devices are bumped or pressed against the tray. If products will be baked while in a tray container, be sure to use a heat-proof tray (trays that are not heat-proof cannot be used for baking). Make sure the tray is labeled either as “HEAT-PROOF” or as “135°C MAX (heat-proof temperature)”. The baking conditions differ according to the product, so check the product specifications to avoid setting too high a baking temperature.

(2) Taped products
The adhesive (non-peeling) strength of tape is affected by storage temperature and humidity conditions. The tape's adhesive must therefore be considered when transferring taped products to a mounting machine. In cases where mounting of products from adhesive tape is stopped and the remaining products are to be stored, avoid winding the tape too tightly, as it may cause some products to come loose from the tape.

(3) Products in magazine container
Be sure to use an anti-static agent on the magazine's outer material. Avoid excessive scraping or rinsing of the magazine's surface, which can remove the anti-static agent or reduce its effectiveness.
These storage cases are designed to be re-used and recycled. Therefore, both during and after use of the magazine container, be careful to protect it from damage and dirt while handling it. Re-using and recycling these containers is one way to reduce their environmental impact.

Use cases provided by Compound Semiconductor Devices Division when products must be divided among several cases. If these cases cannot be used, note the following cautions when selecting the cases to be used.

<1> Avoid materials that may cause chemical reactions or that may emit toxic gas.

<2> Make sure that the case is designed with a stable structure that can withstand vibration and shock without damaging the semiconductor devices it contains.

<3> Use a conductive or static-proof material (such as by coating the material’s surface with anti-static agent to protect product quality) in all parts of the case that come in contact with device pins.
6.3.2 Cautions on packing boxes

Semiconductor devices that are packed into cases must be wrapped in packing material to prevent exposure to external factors such as shock, rain, or dirt. Figure 6-16 shows typical examples of packing used at Compound Semiconductor Devices Division.

Figure 6-16. Examples of Packing Boxes

Once packed into their individual containers, several (up to several dozen) containers can be packed into individual packing boxes. In turn, several (up to several dozen) of these individual packing boxes can be packed into an outer packing box. The outer packing boxes should be secured with plastic adhesive tape. The following are some packing-related cautions.

<1> To minimize exposure of the semiconductor devices to shock, vibration, and/or humidity, ample measures to ensure resistance to shock, vibration, and humidity must be implemented as part of the packing, storing, and shipping methods. Ordinarily, polyfoam or plastic bubble wrap should be placed around the product containers before they are packed into individual packing boxes. After the individual packing boxes are packed into outer packing boxes, use plastic tape or string to secure the flaps of the outer packing boxes. Stronger boxes may be required when storage or shipping conditions are especially rough.
<2> Attach labels (This Side Up, Fragile, Keep Dry, Stack Limit, etc.) (see Figure 6-17) to prevent damage to the contents. Also, attach “Avoid Static Electricity” labels to boxes that contain products that are sensitive to electrostatic discharges.

<3> Seal outer packing boxes in plastic or other air-tight material if the boxes are likely to undergo harsh environmental conditions, such as when shipped by sea.

Figure 6-17. Labels Attached to Boxes

![Labels Attached to Boxes Diagram]
6.3.3 Cautions on storage

When storing semiconductor devices, care is required not only concerning the storage environment and storage method but also, in the case of long-term storage, special care is needed to maintain and confirm product quality.

(1) Storage environment

To maintain the quality of semiconductor devices in storage, the storage environment must be controlled in terms of temperature and humidity and the presence of hazards such as corrosive gas, radioactive rays, and static electricity. (See Figure 6-18.)

Figure 6-18. Cautions on Storage Sites

<1> Maintain the storage site's temperature (T_A) within 5 to 30°C and the humidity (RH) within 20 to 70%.

Also note the following points:

- Use a humidifier in dry regions. In this case, use demineralized water or distilled water for humidifying.
- Avoid storing semiconductor devices in an overheated area, such as an area exposed to direct sunlight or near a heater, since overheated conditions may result in warping of product containers (magazines, etc.).

<2> Store semiconductor devices in areas where temperatures do not fluctuate widely (such as in direct sunlight areas or dark areas), since rapid changes in temperature can cause moisture condensation on the devices.

<3> Store semiconductor devices in an area where the air is clean and free of excess salt, dust, or corrosive gases (such as exhaust gas, smoke, nitrous oxides, sulfur oxides, etc.).

<4> Store semiconductor devices in an area that they will not undergo mechanical stresses such as vibration or shock.

<5> Store semiconductor devices in an area that where they will not be exposed to radioactive rays, static electricity, or strong magnetic fields.
(2) Storage methods

Note the following cautions on semiconductor device storage methods in order to maintain the quality of semiconductor devices. (See Figure 6-19.)

Figure 6-19. Cautions on Storage Methods

<1> Avoid stacking heavy items on top of semiconductor device boxes since the devices may become damaged (cracks, bent leads, etc.). Since stacking boxes adds an undetermined amount of weight, avoid stacking heavy boxes on top of lighter boxes.

<2> Do not allow any vibration or shock that is strong enough to dent the exterior boxes.

<3> Leave lead ends on external pins of semiconductor devices unprocessed to avoid defects that can occur during solder mounting due to rust, etc.
(3) Long-term storage

When storing semiconductor devices for a long period (two years or longer), the following cautions should be noted in addition to the caution points mentioned for “(1) Storage environment” and “(2) Storage methods” above. (See Figure 6-20.)

<1> If long-term storage is expected from the start, use either dry pack or a sealed container that also contains silica gel desiccant. After opening a dry pack package, put the contents back into a dry pack to ensure a long shelf life.

<2> If a long period (two years or longer) has elapsed for semiconductor devices that have been stored under in a normal storage environment and using normal storage methods, we recommend checking for solderability and rust on pins before using the semiconductor devices.

Figure 6-20. Cautions on Long-Term Storage
6.3.4 Cautions on shipping

Note the following cautions concerning shipping of semiconductor devices.

<1> Observe the packaging labels and make sure the boxes are set in a correct position during shipment. Placing boxes upside down or in a leaning position can create unnatural stresses and cause damage. (“This Side Up” label.)

<2> The leads on semiconductor devices can become damaged when a box, dry pack, or tray containing them is dropped, even when no damage is visible on the box, dry pack, or tray. Therefore, be extra careful to avoid dropping storage items when handling them. (“Fragile” label)

<3> Be extra cautious when shipping in rainy or snowy weather so as to prevent seepage of moisture into semiconductor device containers. (“Keep Dry” label)

<4> Be careful to minimize mechanical vibrations and shocks when transferring semiconductor devices.

<5> Keep semiconductor devices and containers out of direct sunlight.

<6> Watch out for temperature rises during shipment.

<7> Condensation may occur on semiconductor devices when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.
6.4 Cautions on ESDs (Electrostatic Discharges)

6.4.1 Mechanisms of ESD-related degradation and damage in semiconductor devices

(1) Mechanism of ESD

Static electricity is an electrical charge that is created when an object has either a surplus or lack of electrons. When two objects come into contact (even if they are electrically neutral) and rub against each other, electrons are transferred from the surface of one object to the surface of the other object, causing the occurrence of positive static electricity in one object and negative static electricity in the other object. When a charged object approaches another object, inductance of static electricity causes static electricity to occur in the object. The amount of electrical charge in a charged object differs greatly depending on the object's type and the conditions of contact and/or friction. Also, since static electricity charges occur on the surfaces of objects, the amount of the charge greatly depends on each surface’s electrical conductivity. Generally, objects made of plastic and chemical fibers which have high insulating characteristics can carry a large electrostatic charge, but the conductivity on the surface of such objects is increased when the objects are in highly humid environment, and this tends to reduce the electrostatic charge. Conductive objects also tend to become electrostatically charged more easily due to their electrostatic induction.

The amount of static electricity can be expressed not only in terms of the amount of electrostatic charge in an object but also in terms of other physical quantities such as the electrostatic potential and the discharge energy. Table 6-2 lists some typical examples of how static electricity is generated.

<table>
<thead>
<tr>
<th>Source of Static Electricity Generation</th>
<th>Electrostatic Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>When RH = 10 to 20%</td>
</tr>
<tr>
<td></td>
<td>When RH = 65 to 90%</td>
</tr>
<tr>
<td>Walking on carpet</td>
<td>35000 V</td>
</tr>
<tr>
<td>Walking on vinyl floor</td>
<td>12000 V</td>
</tr>
<tr>
<td>Working at workbench</td>
<td>6000 V</td>
</tr>
<tr>
<td>Vinyl cover on document</td>
<td>7000 V</td>
</tr>
<tr>
<td>Polyvinyl bag picked up from bench</td>
<td>20000 V</td>
</tr>
<tr>
<td>Seat covered with polyurethane foam</td>
<td>18000 V</td>
</tr>
</tbody>
</table>

(From MIL-HDBK-263)
(2) Mechanism of electrostatic charge, degradation, and damage in semiconductor devices

Static electricity occurs in many kinds of environments that may exist when semiconductor devices are being handled. Accordingly, electrostatic charges can be caused by semiconductor devices touching each other or rubbing against each other or when they are electrostatically inductive.

At semiconductor device fabrication processes and assembly processes, operations such as marking, inspection, conveyance, packaging, and equipment assembly require that semiconductor device packages or lead frames come into contact with (or rub against) other devices or human hands.

When a semiconductor device fabrication equipment unit, electronic equipment assembly unit, jig, tool, or human body touches (either directly or via a conductor) the lead frame in a semiconductor device, the semiconductor device becomes charged and is then susceptible to degradation or damage. (This refers to the Machine Model (MM) and the Human Body Model (HBM).)

When a plastic package rubs against or otherwise comes into contact with or approaches a charged object, a charge occurs on the package's surface due to electrostatic induction. This charge on the package's surface enters via induction or conduction to the chip or lead frame in the package, so that the lead frame discharges when it touches another conductor, which can cause degradation or damage in the device. (This refers to the Charged Package Model).

Semiconductor device damage that is caused by static electricity tends to occur as damage in PN junctions, oxide layers, or wiring. PN junction damage and wiring damage are caused by the discharge energy and oxide layer damage is caused by the amount of electrostatic charge.

As semiconductor devices become more advanced both functionally and in terms of performance, miniaturization of chip structures and higher integration of components has led to increasingly thinner oxide layers and wiring films, which has substantially reduced semiconductor devices’ resistance to electrostatic damage. To make semiconductor devices more robust, semiconductor device manufacturers have implemented various design measures, such as adding static electricity protection circuits to semiconductor devices. These types of design measures may affect the devices’ operating characteristics and cause poor performance, so in some cases it is not possible to insert protection circuits.

Both at semiconductor fabrication processes and at customers’ electronic equipment assembly processes, it is impossible to prevent degradation or damage to semiconductor devices unless static electricity is kept under control.

Compound Semiconductor Devices Division keeps its customers informed of the latest design methods and other new techniques for controlling static electricity at semiconductor device fabrication, inspection, storage, and conveyance processes.

Customers are asked to note the following handling-related caution points whenever they accept semiconductor devices, assemble them into electronic equipment, or inspect them. They are also asked to plan effective countermeasures against static electricity.
6.4.2 Basic methods for preventing ESD when handling semiconductor devices

To prevent degradation and other damages to semiconductor devices that can be caused by electrostatic discharges, electrification of objects must be thoroughly suppressed in any environment in which semiconductor devices are handled.

The basic methods for doing this include suppressing the occurrence of static electricity whenever possible and enabling any electrostatic charge that does occur to be safely discharged.

Five basic methods for controlling ESD while handling semiconductor devices are described below.

<1> Use grounding and avoid using insulating materials on all objects (including human bodies) that touch or approach semiconductor devices. To avoid buildup of electrostatic charges, it is better to use a conductive material that has a high resistivity or a semi-conductive material rather than an insulating material. Grounding is necessary to provide a safe discharge route for electrostatic charges.

<2> Whenever possible, do not allow semiconductor devices to rub against each other or against other objects. Such friction is a cause of electrostatic generation.

<3> Do not approach or touch a charged body (including human bodies). This helps to prevent induction of electrostatic charges from charged bodies to semiconductor devices.

<4> Avoid rapid discharges. To do this, make sure that all objects that may come in contact with semiconductor devices are covered in conductive material that has a high resistivity value. In the case of metal objects, such objects should be grounded via a series resistor with a high resistance value. Rapid electrostatic discharges from semiconductor devices can degrade or damage them.

<5> Do not allow the ambient humidity to fall below 40%. Electrostatic charges occur more easily at lower humidity levels, and this tendency increases rapidly when the humidity level drops below 40%. This is because electrical conductivity on the surface of objects decreases at lower humidity levels, making it easier for a charge to accumulate on an object's surface.

6.4.3 ESD-related cautions on handling of semiconductor devices

First, it is important to implement the five basic methods (see 6.4.2 above) for controlling static electricity in work environments in which semiconductor devices are stored, conveyed, accepted, mounted, or inspected. It is also important to measure and understand the conditions and causes of the occurrence of static electricity and to take appropriate measures.

The following are general anti-static measures that are based on the above-mentioned five basic methods for preventing degradation or damage that can occur in semiconductor devices due to electrostatic discharges when the devices are being handled.

(1) Storage and conveyance

<1> Use anti-static conductive gloves, conductive plastic containers, conductive magazine cases, conductive racks, etc. when storing or conveying semiconductor devices or PCBs on which such devices have been mounted. When packing, storing, or conveying such devices, avoid using insulating plastic containers that facilitate buildup of electrostatic charges, such as vinyl bags, polyethylene containers, and styrofoam boxes.

<2> To prevent storage containers for semiconductor devices or PCBs on which such devices have been mounted from rattling around (i.e., receiving vibration and friction) inside outer boxes during shipment, use containers that are designed for a tight fit and/or insert padding to prevent shifting of contents. This will help to prevent static electricity that can be generated by friction between devices or PCBs and their containers as they are being shipped.

<3> Store the devices on special anti-static storage shelves (shelves that are grounded via a high resistance value of about 1 MΩ).

<4> Attach grounding chains to conveyance carts, vehicles, etc.
<5> Use aluminum foil or a shorting bar to short the connectors of PCBs on which semiconductor devices have been mounted. (See Figure 6-21.)

<6> Use a conductive sheet to cover PCBs on which semiconductor devices have been mounted or a place a conductive mat in front of such PCBs.

Figure 6-21. Example of Antistatic Protection Methods for PCBs
(2) Environment, equipment, tools, and jigs

<1> Maintain the RH between 40% and 60%.
   Use a humidifier to avoid excessively low humidity conditions when in dry regions (or dry seasons). If a
   humidifier alone is not sufficient, use an ionizer also.

<2> Minimize drafts.
   If drafts cannot be eliminated, use an ionizer.

<3> To eliminate sites where static electricity can accumulate, make sure that various devices including
   measuring equipment, test equipment, conveyers, work table, floors, tools, solder baths, soldering irons are
   all grounded. Put high-resistance conductive mats (rated between $10^5$ Ω/γ and $10^9$ Ω/γ) down on work tables
   and floors and make sure each mat is grounded. (See Figure 6-22.)

<4> On equipment used to mount or test semiconductor devices on PCBs, all parts of the equipment that may
   come into contact with semiconductor devices should be made of conductive material or high-resistivity
   conductive material and should be grounded. If insulating materials that are susceptible to static electricity
   buildup are used (making it difficult for static electricity to be discharged), use of an ionizer-equipped air
   blower can be an effective countermeasure.

<5> Select jigs and tools that are treated with semi-conductive material that does not easily build up an
   electrostatic charge and does not rapidly discharge. If a metal jig or tool must be used, ground the jig or tool
   via a resistor with a high resistance value.

<6> Use a semiconductor-type soldering iron (low voltage type, 12 V to 24 V) and connect a grounding source to
   the tip of the iron via a series resistor connection rate at about 1 MΩ. (See Figure 6-23.)

<7> Do not use any other materials that are likely to be sources of static electricity.

Figure 6-22. Anti-Static Measures for Work Area

Figure 6-23. Grounding of Soldering Iron
(3) Staff

<1> Anyone who is handling semiconductor devices, mounting them on PCBs, or testing or inspecting PCBs on which semiconductor devices have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ. (See Figure 6-24.) Grounding of human bodies is an effective method for preventing electrostatic buildup in human bodies and electrostatic damage to devices that such buildup can cause. However, this method is hazardous in that it can amplify the effects of any electrical discharge felt by persons wearing anti-static bands. To avoid this hazard, be sure to insert a series of resistors between the body and the grounding source. The amount of resistance should be determined based on the amount needed as an anti-static measure and the amount needed to protect people from electrical shocks. If a person receives an electrical shock when the resistance value is too low, the person may receive a large current, but too high a resistance value degrades the grounding effect. Therefore, a resistance value of about 1 MΩ is recommended. (JEITA standards recommend a value between 250 kΩ and 1 MΩ).

<2> Footwear (shoes, sandals, etc.) should be made of semi-conductive material. The resistance value of footwear should be between 100 kΩ and 100 MΩ. Note, however, that footwear's resistance value varies due to factors such as dirt, friction, and humidity.

<3> Gloves and other work clothes should be made of non-static cotton or anti-static semi-conductive chemical fibers (resistance: $10^9$ Ω to $10^{14}$ Ω). Avoid using nylon or other easily charged insulating fabric.

Figure 6-24. Body Grounding
(4) Work methods

<1> As for supplies kept in the work area, avoid using easily charged insulating objects (such as objects made of chemical fibers or plastic) and instead use conductive items that have a high resistance value.

<2> The containers used to store or transport semiconductor devices in the work area should be made of anti-static treated material or semi-conductive material (such as static-shield backing).

<3> At PCB assembly processes, make semiconductor devices the last components to be assembled whenever this is possible.

<4> Train operators to touch a grounded work table before starting an operation, or have them use an ionizer to remove electric charges before starting work.

<5> Do not directly touch semiconductor device leads or PCBs on which semiconductor devices are mounted. Use gloves made of cotton to carry semiconductor devices and PCBs.

<6> When mounting devices on PCBs, try to minimize the number of times each device is handled as well as how long it is handled. Working quickly and efficiently is an important way to prevent damage to devices and PCBs.

<7> Be sure to shut off the power before attaching a connector to connect a PCB on which semiconductor devices have been mounted. This prevents abnormal voltage from being applied to devices, which can damage them.

To make the above anti-static measures more effective, we recommend that electrostatic charges be measured at various places where semiconductor devices are handled.
6.5 Cautions on Latchup

It is known that CMOS ICs are susceptible to abnormal operation or damage due to latchup phenomena. The mechanism behind latchups and latchup countermeasures in terms of resistance testing and device design were described in “CHAPTER 3.2 Principal Failure Modes and Failure Mechanisms”. Some use-related caution points are given below.

To prevent latchups in sets that contain CMOS ICs, countermeasures similar to those described in 6.2.3 (1) General cautions are required.
6.6 Measurement-Related Cautions

6.6.1 Cautions on use of IC testers
The caution points concern the use of IC testers for IC acceptance inspections.

(1) Sequence of voltage application to power supply pins and input pins
Voltage should always be applied to ICs via power supply pins. When voltage is applied via input pins prior to applying voltage via power supply pins, current will flow via the pins’ protection circuits, causing latchup. Figure 6-25 shows the structure of a CMOS input protection circuit. When a voltage is applied to input pin $I_1$ before it is applied to the power supply pin $V_{DD}$, a forward bias occurs between the drain (P-type diffusion layer) and the well (N-type diffusion layer) for P-channel transistor $T_1$, which triggers latchup.

![Figure 6-25. Structure of CMOS Input Protection Circuit](image)

(2) I/O switching
When in input mode, a voltage is applied from the IC tester. When in output mode, the tester measures the IC’s output voltage. However, if the I/O switching timing is skewed between the IC and the IC tester, the IC may still output a voltage but voltage may also be applied from the tester, resulting in a large current that may damage the IC (see Figure 6-26). In particular, the address output and the instruction code or data input is repeated on the address/data bus, which means that caution is needed to ensure correct timing in I/O switching. Check the individual data sheet for each device since the I/O timing varies among different devices.

![Figure 6-26. I/O Switching Modes](image)
(3) When using several power supply sources
ICs that have an on-chip A/D converter or analog comparator may include several power supply pins in addition to the main power supply pin (V_{DD}), such as an analog power supply pin (AV_{DD}) or a reference voltage pin (V_{REF}). (see Figure 6-27.)
In such cases, if the AV_{DD} or V_{REF} voltage is several volts greater than the V_{DD} voltage, latchup may be triggered by a large current entering the protection circuits. The protection circuits for AV_{DD} and V_{REF} pins are similar to the protection circuits for input pins that were described in (1) above. Caution is required when changing the power supply voltage during testing.

![Figure 6-27. Example of Multiple Power Supply Sources](#)

(4) Overshoot, undershoot, and spike noise

<1> Power supply voltage overshoot
When an overshoot occurs in the power supply voltage supplied from the IC tester, an overvoltage is applied to the IC, which may damage the IC.

<2> Overshoot and undershoot of signal voltage
When an overshoot or undershoot occurs in the signal voltage applied to input pins, a current flows across the IC’s on-chip protection circuits, causing latchup.
An overshoot causes a current to flow from the P-channel transistor T_1’s drain to the power supply pin V_{DD} and an undershoot causes a current to flow from the N-channel transistor T_2’s drain to the GND pin. (see Figure 6-25 above.)

<3> Spike noise
If spike noise occurs in the power supply voltage and signal voltage applied by the IC tester, the IC may be destroyed depending on the peak voltage. Note that even if the IC is not destroyed, it may still be damaged or its reliability may be degraded.

Since overshoot, undershoot, and spike noise have a powerful effect on the reliability of ICs, it is important to check the voltage waveform to ensure that overshoot, undershoot, and spike noises do not occur.
When using an IC tester, it is very important to properly maintain and carefully program it.
6.6.2 Cautions on probing during inspections and adjustments

When using an oscilloscope probe while inspecting or adjusting assembled printed circuit boards, be careful to avoid shorting the IC's pins. Shorting the pins not only causes operation faults but also can lead to overcurrents which can damage the IC.

1. Check for wiring faults, solder bridges, and other causes of pin shorting before applying a voltage for testing the printed circuit board by applying a voltage.

2. Do not directly probe the IC pins: instead, set up a dedicated test pin. However, the wiring should be kept short enough to prevent electrostatic induction and electromagnetic induction and the wiring capacitance should be kept low. Avoid the use of long wiring to facilitate measurement.

3. When using a board check tester, note the same caution points (described above) as when using an IC tester.

4. Connect unused input pins to VDD or GND to lower the input impedance. Although leaving some unused input pins unconnected may afford more flexibility for making design changes, it is not advisable because it reduces anti-noise protection.
6.7 Cautions on Device Mounting

This section explains the recommended soldering conditions of Compound Semiconductor Devices Division's products.
For the detailed information on mounting methods of SMD and THD packages, related points to be noted, flux type, and cleaning conditions, please inquire of Compound Semiconductor Devices Division's salesperson.

6.7.1 Recommended soldering conditions

(1) Compound Semiconductor Devices Division’s concept of recommended conditions

Compound Semiconductor Devices Division specifies recommended soldering conditions for each of its products.
This is because the quality of each SMD is affected to varying degrees by the following three factors.
<1> Moisture absorption of package (storage conditions)
<2> Soldering conditions (method and conditions)
<3> Package structure (thickness, chip size, etc.)

Therefore, Compound Semiconductor Devices Division specifies recommended soldering conditions for each product without categorizing products into groups of products and packages.
For details of the recommended soldering conditions for a particular product, contact your local Compound Semiconductor Devices Division sales representative.

(2) Categories of recommended soldering conditions

Compound Semiconductor Devices Division’s recommended soldering conditions can be broadly divided into:
<1> heating conditions of soldering method; <2> package moisture absorption control; and <3> number of times the product is to be mounted.

Figure 6-28 shows basic soldering temperature profiles recommended by Compound Semiconductor Devices Division. The classification of soldering methods and the recommended soldering conditions are shown in Table 6-3.
Table 6-3. Recommended Reflow Soldering Conditions of Surface Mount Components

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Preheating</th>
<th>Heating</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt;1&gt; Temperature Range</td>
<td>&lt;2&gt; Time</td>
</tr>
<tr>
<td>IR215</td>
<td>130 to 160°C</td>
<td>70 to 150 s</td>
</tr>
<tr>
<td>IR230</td>
<td>120 to 150°C</td>
<td>60 to 120 s</td>
</tr>
<tr>
<td>IR235</td>
<td>100 to 160°C</td>
<td>60 to 120 s</td>
</tr>
<tr>
<td>IR260</td>
<td>120 to 180°C</td>
<td>90 to 150 s</td>
</tr>
</tbody>
</table>

Notes 1. The recommended peak temperature for infrared reflow soldering is 215°C, 230°C, 235°C, or 260°C, depending on the product. For details, contact your local Compound Semiconductor Devices Division sales representative.

2. The number of times the product can be mounted is once, twice or three times depending on the product. For details, contact your local Compound Semiconductor Devices Division sales representative.

3. For details on the partial heating method, refer to the Compound Semiconductor Devices Division's website (Where to find this manual, [Top Page] > [Environmental Activities] > [Pb-Free]). If using a soldering iron method or wave soldering method, be sure that the soldering equipment is free of commercial power supply leakage and that it is grounded via a resistance of about 1 MΩ.
(3) Symbol codes used in descriptions of recommended soldering conditions

The symbol codes that indicate Compound Semiconductor Devices Division's recommended soldering conditions include codes indicating: <1> heating conditions of each soldering method; <2> package moisture absorption control, and <3> the maximum number of mounting times.

In addition, there are symbol codes which indicate the soldering method, peak temperature, baking time and the number of storage days after the dry pack has been opened, and the maximum number of mounting times. These symbol codes are used in the following combinations. Figure 6-29 shows examples of symbol codes for recommended soldering conditions.

![Figure 6-29. Symbol Codes for Recommended Soldering Conditions](image-url)
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A.1 What Is Sampling Inspection?

Sampling inspection is a type of inspection that is performed on sample products which are randomly selected from a lot. The entire lot is either accepted or rejected based on the results of sampling inspection. In other words, this type of inspection allows certain amounts of risk: the producer's risk (probability $\alpha$) that a nondefective lot may be rejected and the consumer's risk (probability $\beta$) that a defective lot may be accepted. Sampling inspections are the norm for semiconductor devices; full-lot inspections are not feasible since breakdown tests are sometimes required as reliability tests and lot sizes tend to be rather large.

This appendix describes the quality control type of sampling inspections that are performed as shipment inspections, and also briefly describes sampling inspections that are performed as part of reliability testing.

(1) OC curve

Given "N" as the lot size, "p" as the defect rate, "n" as the number of samples taken from the lot, and "x" as the number of defective items among the samples, it is possible to calculate the probability of defectives as $P(x)$. A hypergeometric distribution, binomial distribution, or Poisson distribution (see APPENDIX B) can be extracted based on factors such as the lot size. The following is a Poisson distribution.

$$P(x) = e^{-pn} \frac{(pn)^x}{x!}$$

The acceptance ($\alpha$) or rejection ($\beta$) probability is expressed as follows.

$$1-\alpha = 1-L(P_0)$$
$$\beta = L(P_1)$$

Figure A-1 shows an OC curve that describes quality characteristics (such as the defect rate) by using the acceptance probability as its vertical axis and the rejection probability as its horizontal axis.
The above diagram is called an “Operating Characteristic curve”, or “OC curve” for short. One OC curve can be obtained for each condition that is established for the sampling inspection system. OC curves provide information that indicates the probability of acceptance or rejection for a lot having a certain quality characteristic.

For example, during single sampling inspection by attributes based on operating characteristics (as defined by JIS Z 9002), if \( P_0 = 1.0\% \) and \( P_1 = 5.0\% \), then \( n = 120 \) and \( C = 3 \). The corresponding OC curve is shown in Figure A-2, and the lot acceptance probability can be interpreted as shown below.

If \( p = P_0 = 1.0\% \), then \( L(P_0) \approx 0.97 \)

If \( p = P_1 = 5.0\% \), then \( L(P_1) \approx 0.14 \)

**Figure A-2. OC Curve When \( P_0 = 1\% \) and \( P_1 = 5\% \)**

In other words, this curve indicates that there is a 0.03 producer’s risk (probability \( \alpha \)) that a nondefective lot having defect rate \( P_0 \) will be incorrectly judged as a rejected lot, or there is a 0.14 consumer’s risk (probability \( \beta \)) that a defective lot having defect rate \( P_1 \) will be incorrectly judged as an accepted lot.

The effectiveness of sampling curves is determined based not only on OC curves; it also depends greatly on the inspected lot’s average defect rate and the amount of variation reflected in the rate.

(2) **Types of sampling inspections**

The following are some types of sampling inspections.

- Sampling inspection by attributes or by variables
- Sampling inspection based on operating characteristics, screening, adjustments, or continuous production
- Single, double, multiple, or sequential sampling inspection

For example, JIS Z 9002 describes single sampling inspection by attributes based on operating characteristics. Below, AQL and LTPD methods are briefly explained as two of the many sampling inspection methods.
(3) AQL and LTPD

The AQL (Acceptable Quality Level) is established based on an OC curve which describes the probability \((1 - \alpha)\) that a lot having defect rate \(P_0\) will be accepted. This method is part of the sampling inspection by attributes based on operating characteristics defined in MIL-STD-105 and JIS Z 9015. The severity of sampling inspections is adjusted among the following three severity levels, according to quality level factors such as past lot inspection results.

- Normal level: Quality level has been generally near the AQL.
- Tightened level: Quality level has been clearly worse than the AQL.
- Reduced level: Quality level has been generally above the AQL and is expected to remain above the AQL.

In addition, an inspection level is established based on the relation between the lot size and the number of samples (i.e., the proportional inspection volume). The inspection level is also established based on other factors, such as inspection costs and consistency of quality within and between lots. Although there are seven inspection levels, including ordinary inspection levels I to III and special inspection levels S-1 to S-4, general level II is generally used unless a special level is specified.

The AQL resembles the defect rate \((P_0)\) used in OC curves in that both refer to a threshold value of quality as a criterion for accepting or rejecting sampled lots. However, AQL differs from \(P_0\) in the following ways.

1. \(P_0\) refers to an individual lot, while AQL refers to an average for a process.
2. \(P_0\) indicates one point on an OC curve as an attribute combined with the producer’s risk \((\alpha)\) but this \(\alpha\) value changes according to factors such as lot size when AQL is used instead of \(P_0\).

Example: At this time, given a lot size of 5000 and an AQL of 0.65, a 200-unit sample, \(Ac = 3\), and \(Re = 4\) is taken. The lot is accepted if there are no more than three defectives in the sample (the “acceptance number”) and is rejected if there are four or more defectives (the “rejection number”).

The LTPD (Lot Tolerance Percent Defective) is established based on an OC curve which describes the probability \((1 - \beta)\) that a lot having defect rate \(P_1\) will be rejected. For example, MIL-S-19500 and other standards define single sampling inspection by attributes based on exponential distribution (MIL-S-19500 uses \(\beta = 0.1\) as the probability). Consequently, LTPD is the defect rate for an inspection lot for which the acceptance probability in sampling inspections is \(\beta = 0.1\), which corresponds to \(P_1\) on an OC curve.

The LTPD sampling table shown below was calculated based on a Poisson distribution and can be used when the lot size \((N)\) is at least 200. Therefore, for lot sizes of less than 200, a sampling table calculated based on a hypergeometric distribution must be used.

The table's horizontal axis shows LTPD values (unit percentages), but when implementing a sampling inspection based on failure rates these values can also be viewed as lot tolerance failure rates (unit percentage divided by 1000 hours). However, when implementing a sampling inspection based on failure rates, the minimum number of defective units as read from the LTPD sampling table can be replaced by a component hour value (acceleration coefficient \(\times\) units \(\times\) time) that is 1,000 times greater.

Example: To guarantee (using “1” as the acceleration coefficient) the results of 1000 hours of testing in which the lot sizes were established as more than 200 units and in which \(\lambda = 1\% / 1000\) hours, if the acceptance number \((C)\) is 0, a sample size \((n)\) of 231 units is required.
(4) Sampling tests as part of reliability testing

There is no substantial difference between sampling tests performed as part of reliability testing and sampling tests performed as part of quality control. The main differences are explained below.

<1> Scale Reliability: Failure rate ($\lambda$), MTBF, etc.
Quality control: Defect rate ($p$)

<2> Distribution Reliability: Mainly uses exponential distribution
Quality control: Normal distribution

<3> When used for reliability testing, sampling tests are sometimes cut short since a lot of time is needed to check failures in all sample units.

$\lambda_0$: Acceptable quality level
ARL: Acceptable Reliability Level
AFR: Acceptable Failure Rate
$\lambda_1$: LTFR (Lot Tolerance Failure Rate)
$\alpha$: Producer's risk ($1 - \alpha$ = lot acceptance rate)
$\beta$: Consumer's risk
$\lambda_0/\lambda_1$: Discrimination ratio (normally selectable between 1.5 and 3.0).

Example: Let us consider a fixed time single sampling LTFR method (repair-related). Total test period: if $k$ times is the number of failures for $nT$, the acceptance rate can be determined as shown below.

$$Pr(x) = \frac{(n\lambda T)^x}{x!} e^{-n\lambda T}$$

$$L(p_c) = \sum_{k=0}^{c} \frac{(n\lambda T)^x}{k!} e^{-n\lambda T}$$

$$= \int_{2n\lambda T}^{\infty} g_{\chi^2(c+1)}(\zeta)d\zeta$$

The last term in the above expression is the density function of a chi-square distribution of degree of freedom 2 ($c + 1$). The following establishes $L(\lambda)$ as less than $\beta$.

$$2n\lambda T > \chi^2(2(c + 1), \beta)$$

Consequently, $T$ must be obtained to satisfy the above expression.

Given $n = 10$, $\beta = 0.1$, $\lambda = 0.001$, and $c = 0$:

$$\chi^2(2(0 + 1), 0.1) = \chi^2(2, 0.1) = 4.61$$

$$T = \frac{4.61}{2 \times 10 \times 0.001} = 231$$

Thus, the lot is accepted if no failures occur during 231 hours of testing.
A.2 AQL Sampling Table (MIL-STD-105)

Table A-1. Sample Size Code Letters

<table>
<thead>
<tr>
<th>Lot Size</th>
<th>Special Inspection Level</th>
<th>General Inspection Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S-1</td>
<td>S-2</td>
</tr>
<tr>
<td>2 – 8</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>9 – 15</td>
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<td>16 – 25</td>
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<td>26 – 50</td>
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<td>B</td>
</tr>
<tr>
<td>51 – 90</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>91 – 150</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>151 – 280</td>
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<td>C</td>
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<td>281 – 500</td>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>501 – 1200</td>
<td>C</td>
<td>C</td>
</tr>
<tr>
<td>1201 – 3200</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>3201 – 10000</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>10001 – 35000</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>35001 – 150000</td>
<td>D</td>
<td>E</td>
</tr>
<tr>
<td>150001 – 500000</td>
<td>D</td>
<td>E</td>
</tr>
<tr>
<td>500001 and over</td>
<td>D</td>
<td>E</td>
</tr>
</tbody>
</table>

**Note**  MIL-STD-105 is replaced by NSI Standard ANSI/ASQC Z 1.4.
# Table A-2. Single Sampling Plan for Normal Inspection (Master Table)

<table>
<thead>
<tr>
<th>Sample Size Code Letter</th>
<th>AQL (Normal Inspection)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.010 0.015 0.025 0.040 0.065 0.10 0.15 0.25 0.40 0.65 1.0 1.5 2.5 4.0 6.5 10 15 25 40 65 100 150 250 400 650 1000</td>
</tr>
<tr>
<td>A</td>
<td>0 1 1 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
</tr>
<tr>
<td>B</td>
<td>0 1 1 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
</tr>
<tr>
<td>C</td>
<td>0 1 1 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
</tr>
<tr>
<td>D</td>
<td>1 2 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
</tr>
<tr>
<td>E</td>
<td>1 2 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
</tr>
<tr>
<td>F</td>
<td>2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
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<td>G</td>
<td>0 1 1 2 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
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<td>L</td>
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</tr>
<tr>
<td>R</td>
<td>0 1 1 2 2 3 3 4 5 6 7 8 10 11 14 15 21 22 30 31</td>
</tr>
</tbody>
</table>

\[\downarrow\] = Use first sampling plan below arrow. If sampling size equals, or exceeds, lot or batch size, do full-lot inspection.

\[\uparrow\] = Use first sampling plan above arrow.

Ac = Acceptance number

Re = Rejection number

MIL-STD-105
Table A-3. Single Sampling Plan for Tightened Inspection (Master Table)

<table>
<thead>
<tr>
<th>Sample Size Code Letter</th>
<th>0.010</th>
<th>0.015</th>
<th>0.040</th>
<th>0.065</th>
<th>0.10</th>
<th>1.0</th>
<th>2.5</th>
<th>4.0</th>
<th>6.5</th>
<th>10</th>
<th>15</th>
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<th>100</th>
<th>150</th>
<th>250</th>
<th>400</th>
<th>650</th>
<th>1000</th>
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<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
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Table A-4. Single Sampling Plan for Reduced Inspection (Master Table)

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↓ = Use first sampling plan below arrow. If sampling size equals, or exceeds, lot or batch size, do full-lot inspection.
↑ = Use first sampling plan above arrow.
Ac = Acceptance number
Re = Rejection number
↑ = If acceptance number has been exceeded, but the rejection number has not been reached, accept the lot, but reinstate normal inspection.
### A.3 LTPD Sampling Table (MIL-S-19500)

#### Table A-5. LTPD Sampling Table (1/2)

Minimum sample size required to guarantee with 90% reliability that lots having the defect rate specified by LTPD (or an equivalent defect rate) will not be accepted.

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<td>(21.18)</td>
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Notes

1. The sample sizes are based on the Poisson binomial distribution exponent's limit.
2. The minimum quality (approximate AQL) required to accept on the average 19 of 20 lots is shown parenthesis for information only.
## APPENDIX A SAMPLING INSPECTION

### Table A-5. LTPD Sampling Table (2/2)

(Single sampling)

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MIL-S-19500

Technical Note PQ10478EJ02V0TN
APPENDIX B  BASIC MATHEMATICS RELATED TO RELIABILITY

B.1  Reliability Scales and Failure Rates

(1) Concept of reliability
Reliability has been defined in JIS Z 8115 (Glossary of terms used in reliability) as characteristics that enable an item to perform its required functions under the stipulated conditions and for the stipulated time period. However, a more concrete and quantitative (rate-based) definition of reliability is needed if this definition is to be applied toward actually calculating the reliability of systems and devices. Japanese standards—specifically, JIS Z 8115 (Glossary of terms used in reliability)—therefore make a distinction between two types of reliability. In contrast to the above qualitative type of reliability (“shinraisei” in Japanese) is a quantitative type of reliability (“shinraido”) defined as the probability that a system, product, or part will perform its stipulated functions (without failures) under the stipulated conditions and for the stipulated time period. It is important to clearly understand the following elements of this definition.

<1> What is the subject?
<2> What are the functions, and what kind of failure results when a function is lost?
<3> What is the stipulated time period?
<4> What are the stipulated use conditions?

Now that the abstract concept of reliability has been redefined as a quantitative rate (probability), it can be used to express the degree of reliability found in systems and devices.

(2) Scales used to express reliability

<1> Reliability function:  \( R(t) \)
After time \( t \) has elapsed, a ratio of devices or equipment units that have not failed is obtained. This ratio is expressed as follows.

\[
R(t) = \frac{n - c(t)}{n}
\]

Where

\( n \): Total sample size
\( c(t) \): Number of failures during time period \( t \)

In other words, 100% reliability occurs when \( R(t) = 0 \), but this percentage is reduced over time as more samples fail and the number of remaining samples gradually approached zero.

<2> Unreliability function:  \( F(t) \)
After time \( t \) has elapsed, a ratio of devices or equipment units that have failed is obtained. This ratio is expressed as follows.

\[
F(t) = \frac{c(t)}{n}
\]

Where

\( n \): Total sample size
\( c(t) \): Number of failures during time period \( t \)

The following relation is established between the reliability function \( R(t) \) and the unreliability function \( F(t) \).

\[
R(t) + F(t) = 1
\]

This relation is illustrated in Figure B-1 below.
In other words, the reliability function $R(t)$ and the unreliability function $F(t)$ are complementary. This means that the number of samples that do not fail can be measured to determine the reliability function and, conversely, the number of samples that fail can be measured to determine the unreliability function.

**<3> Failure density function: $f(t)$**

After time $t$ has elapsed, the ratio of devices or equipment units that fail during a given unit of time is expressed as follows.

$$f(t) = \frac{dF(t)}{dt}$$

Where

$f(t)$: Failure density function

**<4> Failure rate function: $\lambda(t)$**

Among the devices or equipment units that remain after time $t$ has elapsed, the ratio of those that fail during a given unit of time is expressed as follows.

$$\lambda(t) = \frac{f(t)}{1 - F(t)} = \frac{f(t)}{R(t)}$$

This function in this expression is also referred to as the "hazard rate function".

**<5> Cumulative hazard function: $H(t)$**

This function is expressed in an area that is enclosed by the failure rate function $\lambda(t)$ and a time $t$ axis. In other words, it is a cumulative function for the failure rate function $\lambda(t)$, and is expressed as follows.

$$H(t) = \int_0^t \lambda(t)dt$$

If the failure rate is constant random failure, reliability follows an exponential distribution curve. In such cases, the cumulative hazard function $H(t)$ is expressed as follows.

$$H(t) = \lambda t$$

Figure B-2 illustrates the relations among these various functions.
Figure B-2. Relationship Between $F(t)$, $R(t)$, $f(t)$, and $\lambda(t)$

\[ R(t) + F(t) = 1 \]

\[ \lambda(t) = \frac{1}{R(t)} \cdot \frac{dR(t)}{dt} \]

\[ f(t) = \frac{dF(t)}{dt} \]

(3) Failure rates among semiconductor devices

<1> Failure rate patterns

Failure rates can be divided into the following three time-dependent failure rate patterns.

I DFR (Decreasing Failure Rate) pattern
Pattern in which failures decrease over time

II CFR (Constant Failure Rate) pattern
Pattern in which failures are not time-dependent

III IFR (Increasing Failure Rate) pattern
Pattern in which failures increase over time
Figure B-3. Changes in Failure Rates over Time (Bathtub Curve)

Semiconductor devices

Generally, failure rates follow a curve such as the one shown in Figure B-3. This type of curve is called a “bathtub curve” due to its shape, and its time span is divided into three failure stages: the early failure stage, random failure stage, and wear-out failure stage. Ordinarily, defects that occur in the early failure stage are due to manufacturing defects. During this stage, the number of failures starts out high but drops over time until it reaches a stable level. The random failure stage roughly corresponds to the effective life of semiconductor devices. During this stage, the failure rate remains nearly constant. During the wear-out failure stage, the failure rate in certain failure modes begins to increase rapidly, indicating the end of the product’s life. Usually, the wear-out failure stage for semiconductor devices comes long after the end of the useful life of application systems that contain semiconductor devices, so only semiconductor device failures that occur during the early failure stage or random failure stage affect the reliability or maintainability of such application systems.

The semiconductor devices with latent defects that become apparent during the early failure stage can be almost entirely eliminated out by screening processes such as burn-in. Adequate measures are taken at the product design stage to deal with failures during the wear-out failure stage. Consequently, the following are three key points for realizing highly reliable semiconductor devices.

i. Build in reliability at the design stage and confirm it via certification testing.
ii. Build in quality at manufacturing processes.
iii. Use screening processes to eliminate latent defects that would otherwise appear during the early failure stage.

As indicated above, failures among semiconductor devices can be divided into several types, and clarifying failure distribution patterns is an important part of reliability data analysis.
B.2 Probability Distribution for Reliability Analysis

(1) Normal distribution

Normal distribution is the type of distribution that is most frequently used for quality control. The “N” symbol ($\mu$, $\sigma^2$) is used to express it.

This distribution curve is a symmetrical “bell curve” with an average value at the center. Also, 99.73% of the measured time value $t$ is contained in the distance from the average value $\mu$ to $\pm 3 \sigma$ ($\pm$: on both sides of $\mu$), 95.45% is contained in the distance from $\mu$ to $\pm 2 \sigma$, and 68.3% from $\mu$ to $\pm \sigma$.

According to this distribution curve, the times when failures occur are concentrated in the middle of the curve and correspond to the wear-out failure stage in the bathtub curve. The failure density function is expressed as follows.

$$ f(t) = \frac{1}{\sqrt{2\pi \sigma}} \exp \left\{ -\frac{(t-\mu)^2}{2\sigma^2} \right\} \quad (-\infty < t < \infty) $$

Where

- $\mu$: Average value
- $\sigma$: Distribution

(2) Logarithmic normal distribution

A logarithmic normal distribution is distribution in which the logarithm int for time $t$ has a normal distribution pattern. For example, distribution patterns for electromigration life or time required for repairs (i.e., maintainability function) are known to be logarithmic normal distribution patterns.

The probability density function $f(t)$ is expressed as follows.

$$ f(t) = \begin{cases} 
\frac{1}{\sqrt{2\pi \sigma t}} \exp \left\{ -\frac{(\ln t - \mu)^2}{2\sigma^2} \right\} & (t > 0) \\
0 & (t \leq 0) 
\end{cases} $$

The pattern of this probability density function $f(t)$ has extreme values at the center and is asymmetrical, but it approximates a normal distribution pattern if the $\sigma$ value is small.
The pattern shows an increase in the failure rate over time.

![Graph showing failure rate over time with different values of σ.](image)

(3) **Exponential distribution**

The failure rate ($\lambda$) has a constant distribution in relation to time, which corresponds to the random failure stage in the bathtub curve. This type of distribution is widely used in reliability analysis of devices and systems.

The probability density function $f(t)$ and the reliability rate $R(t)$ are expressed as follows.

\[
\begin{align*}
  f(t) &= \begin{cases} 
    \lambda \exp(-\lambda t) = \frac{1}{t_0} \exp \left( -\frac{t}{t_0} \right) & (t \geq 0) \\
    0 & (t < 0)
  \end{cases} \\
  R(t) &= \exp(-\lambda t) = \exp \left( -\frac{t}{t_0} \right)
\end{align*}
\]

$\frac{1}{\lambda} = MTTF = t_0$  \text{(Parameters)}

$R(t_0) = \exp(-1) = 0.368$

In contrast to a normal distribution in which most failures are concentrated within $\pm 3 \sigma$ of the average value $\mu$, the reliability rate in this curve is spread out from $t = 0$ toward $\infty$.

Note also that the reliability rate during the average life is only 36.8%, compared to 50% in a normal distribution.

This distribution corresponds to the Weibull distribution described below in cases where the form parameter $m = 1$. 
(4) Weibull distribution

The Weibull distribution was developed by a Swede named Weibull, who first used it to represent the distribution of the breaking resistance of steel. This distribution can be made to correspond to any stage in the whole range of failure distribution, including the early failure stage, random failure stage, or wear-out failure stage, depending on the value selected as the form parameter m. This explains why Weibull distribution is the type of distribution that is most widely used in reliability rate analysis of semiconductor devices.

The failure density function $f(t)$, the reliability rate $R(t)$, and the failure rate $\lambda(t)$ are expressed as follows.

Where

$$f(t) = m \frac{t^{m-1}}{t_0} \exp\left(-\frac{t^m}{t_0}\right)$$

$$R(t) = \exp\left(-\frac{t^m}{t_0}\right)$$

Where

$m$: Form parameter

$\lambda(t) = m \frac{t^{m-1}}{t_0}$

In this case, the distribution pattern is determined by the value of the form parameter m.

When $m = 1$

The failure rate $\lambda(t)$ is constant, which indicates random failures. This also matches the exponential distribution.

When $m > 1$

The failure rate $\lambda(t)$ increases over time, which indicates wear-out failures. The failure density function $f(t)$ approximates the pattern of logarithmic normal distribution when $m = 2$ and it approximates the pattern of normal distribution when $m = 4$.

When $m < 1$

The failure rate $\lambda(t)$ decreases over time, which indicates early failures.
The analyses described so far presuppose that failures can occur at any time after observations are started. Actually, however, there are certain time periods during which failures are not observed. In such cases, a time factor ($\gamma$) representing the period before the first failure occurs must be introduced to the various expressions related to the above failure distributions, which changes the distribution patterns. The following expression shows how this time factor $\gamma$ is introduced as a position parameter in a Weibull distribution.

$$f(t) = \frac{m(t - \gamma)^{m-1}}{t_0} \exp \left\{ -\frac{(t - \gamma)^2}{2t_0^2} \right\}$$

$\gamma$: Position parameter

For practical purposes, the time factor $\gamma$ represents a failure-free period.

(5) Gamma distribution

A gamma distribution is used to indicate the distribution of failure periods corresponding to cumulative failures that include the cumulative failure period of systems that use parts whose failures fall under an exponential distribution as well as random stress-related failures. The parameters in a gamma distribution are $\lambda$ (scale) and $\kappa$ (form). Like the Weibull distribution, the shape of a gamma distribution curve varies according to the value of form parameter $\kappa$. Analysis using gamma distribution is rather complex, as indicated below, and therefore gamma distribution is seldom used.

$$f(t) = \frac{m^\kappa}{\Gamma(\kappa)}t^{\kappa-1}e^{-mt}$$
(6) Hypergeometric distribution, binomial distribution, and Poisson distribution

The types of distribution described so far mainly have been continuous distributions that indicate failure periods. Hypergeometric distribution, binomial distribution, and Poisson distribution are discrete distributions that mainly indicate numbers of failures.

(a) Hypergeometric distribution

This type of distribution is used to indicate the effects of a relatively small lot size \( N \) on the probability of failures detected during sampling.

\[
f(x) = \frac{n \binom{N-x}{n-N} \binom{N}{n}}{\binom{N}{n}}
\]

(b) Binomial distribution

Since hypergeometric distribution requires some complicated calculations, binomial distribution is used instead when the \( N \) value is sufficiently larger than the \( n \) value (when \( N / n > 10 \)) (i.e., when there is no effect on the failure probability even during multiple sampling).

\[
f(x) = \binom{n}{x} p^x (1-p)^{n-x}
\]

(c) Poisson distribution

This type of distribution is even less difficult than binomial distribution, and it is used when the \( N \) value is sufficiently larger than the \( n \) value and the \( p \) value is small (\( p < 10\% \)).

\[
f(x) = \frac{1}{x!} (np)^x e^{-np}
\]

(7) Chi-square (\( \chi^2 \)) distribution

A chi-square distribution is a distribution in which independent random variables follow a sum-of-squares distribution while each random variable follows its own standard normal distribution. In reliability analysis, when the failure periods follow an exponential distribution, it is known that \( 2^r \) (the total test time before failures occur “r” times) / MTBF follows a chi-square distribution of degree of freedom \( 2r \). This is then used to calculate the failure rate as a constant failure rate or to calculate the number of failure rate sampling tests.

\[
f(\chi^2) = \frac{1}{2^{\nu / 2} \Gamma(\nu / 2)} \left( \frac{\chi^2}{2} \right)^{\frac{\nu - 1}{2}} \exp\left( -\frac{\chi^2}{2} \right)
\]
(8) Summary of distribution functions

Table B-1. Summary of Distribution Functions

<table>
<thead>
<tr>
<th>Distribution</th>
<th>Parameter(s)</th>
<th>Average Value</th>
<th>Dispersion</th>
<th>Median</th>
<th>Mode</th>
<th>Application Example</th>
<th>Life</th>
<th>Other Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exponential</td>
<td>$\lambda$</td>
<td>$1/\lambda$</td>
<td>$1/\lambda^2$</td>
<td>$1n2/\lambda$</td>
<td>0</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Rainfall density</td>
</tr>
<tr>
<td>Weibull</td>
<td>$m, \eta, \gamma$</td>
<td>$\eta\left[1 + \frac{1}{m}\right]^\gamma$</td>
<td>$\eta\left[(1 + \frac{2}{m}) - f(1 + \frac{1}{m})\right]$</td>
<td>$\eta(\ln2)\gamma + \gamma$</td>
<td>$m &gt; 1$</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Tensile strength, Amount of corrosion, Wind speed, Human achievement</td>
</tr>
<tr>
<td>Double exponential (maximum value)</td>
<td>$\mu, \alpha, \gamma$</td>
<td>$\mu + \frac{\gamma}{\alpha}$</td>
<td>$\pi^2 \gamma / 6\alpha^2$</td>
<td>$\mu - \ln2 \alpha$</td>
<td>$\mu$</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Maximum depth of corrosion, Maximum seismic intensity</td>
</tr>
<tr>
<td>Double exponential (minimum value)</td>
<td>$\mu, \alpha, \gamma$</td>
<td>$\mu - \frac{\gamma}{\alpha}$</td>
<td>$\pi^2 \gamma / 6\alpha^2$</td>
<td>$\mu + \ln2 \alpha$</td>
<td>$\mu$</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Breaking resistance of ceramic</td>
</tr>
<tr>
<td>Gamma</td>
<td>$\lambda, \kappa$</td>
<td>$\kappa / \lambda$</td>
<td>$\kappa / \lambda^2$</td>
<td>$\chi^2(2\kappa, 0.5)$</td>
<td>$\kappa &gt; 1$</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Standby time, Rainfall intensity</td>
</tr>
<tr>
<td>Normal</td>
<td>$\mu, \sigma$</td>
<td>$\mu$</td>
<td>$\sigma^2$</td>
<td>$\mu$</td>
<td>$\mu$</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Preventive maintenance period, White noise, DNA distribution</td>
</tr>
<tr>
<td>Logarithmic normal</td>
<td>$\mu, \sigma$</td>
<td>$\exp(\mu + \sigma^2/2)$</td>
<td>$\exp(2\mu + \sigma^2)$</td>
<td>$\exp(\mu)$</td>
<td>$\exp(\mu - \sigma^2)$</td>
<td>$\checkmark$</td>
<td>$\checkmark$</td>
<td>Corrective maintenance period, Density of atmospheric pollution, Size of rain drops</td>
</tr>
</tbody>
</table>

Note:
* $\gamma$: Euler's constant ($= 0.577215...$)
** $\pi$: pi ($= 3.14159...$)
*** $\chi^2(2\kappa, 0.5)$: point indicating upper 50% of chi-square distribution for degree of freedom $2\kappa$;
\(\checkmark\): Applicable
B.3 Failure Models for Accelerated Life Tests

(1) Boundary model and endurance model
A boundary model is a model of how failures suddenly occur when stress is applied to a semiconductor device (or other device) beyond a certain boundary. An endurance model is a model of how failures occur not as soon as stress is applied but rather after stress has accumulated over a certain amount of time. A macro failure model is classified as either a boundary model or an endurance model.

(2) Reaction model
This is a typical type of accelerated life model for semiconductor devices. Generally, any object's destruction or degradation is due to changes that occur at the atomic or molecular level, involving mechanisms such as dispersion, oxidation, absorption, corrosion, and crack length. When such changes progress beyond a certain boundary, a failure occurs. The Arrhenius model is a reaction logic model that is widely used to describe temperature dependence. The reaction speed \( K \) is expressed as follows.

\[
K = A \exp\left(-\frac{E_a}{kT}\right)
\]

Where
- \( A \): constant,
- \( E_a \): activation energy,
- \( k \): Boltzmann's constant,
- \( T \): absolute temperature

Life (\( L \)) is defined as \( L = B/K \) (where \( B \) is a constant).
However, \( \ln L = C + \frac{E_a}{kT} \).

(3) Stress strings model
This is a model of how failures occur when applied stress exceeds a material's strength. Since both the strength and the stress have their own distributions, such failures occur statistically. In the case of semiconductor devices, this model may be used to describe package cracks that occur during reflow soldering of a package that has absorbed some moisture.

One of the characteristics of reliability data is that it is difficult to obtain all of the failure data from the reliability data. Such data is incomplete in almost every case. If failure data taken from such incomplete data is analyzed, there is a risk that the analysis will lead to mistaken judgments. Therefore, this section introduces the Weibull hazard probability paper as a general analytical method that is designed to use incomplete data.

\[
H(t) = \int_0^t \lambda(x)dx \\
R(t) = e^{-\lambda(t)\eta}
\]

A Weibull distribution of the above:

\[
H(t) = \left( \frac{t}{\eta} \right)^m \\
\ln H(t) = m \ln t - m \ln \eta
\]

When these distributions are both entered on logarithmic graphs, we can see a linear relation between them.

As for \(H(t)\), if we use the Kaplan-Meier estimation method, the remaining number \(N_i\) is estimated to become relatively large, as shown below.

\[
N_i = N_1 + N_2 + \cdots + N_i
\]

The steps in this analysis are described below.

Step 1.

It is helpful to use a worksheet, such as the one shown in Table B-2, for this analysis. First, enter the failure period data in ascending order (from smallest to largest values). Next, enter these sample numbers and failure mode or symbol according to the order indicated in the “Order i” column.

Step 2.

Determine the reverse order (\(N_i = n - i + 1\)) and enter each reciprocal number (hazard value: \(h_i\)) in the worksheet.

Step 3.

Add up the hazard values (\(h_i\)) corresponding to hazardous failure modes to obtain a cumulative hazard value (\(H_i\)).

Step 4.

Enter points corresponding to the \(H_i\) value and the failure period data on the probability paper. The points should fall on or near a straight line. Check to make sure there are no singular points. If there is a clear reason for doing so, insert \(\gamma\) (position parameter) to correct the alignment of points (see Figure B-4).

Step 5.

Estimate the parameters.

Draw a straight line parallel to the point where \(\ln t = 1\) and \(\ln H(t) = 0\) (marked as \(\sqrt{\cdot}\)). The \(\ln H(t)\) value is \(m\) at the point where this line intersects the point at which \(\ln t = 0\).

To estimate \(\eta\), read the vertical line that drops below the \(t\) axis from the intersection with the line that corresponds to \(h(t) = 100\%\). If \(\mu\) and \(\sigma\) must also be determined, determine them by reading the scale values at \(\mu / \eta\) and \(\sigma / \eta\) and multiply each of these values by \(\eta\). Refer to the example shown below. You may also want to try out the available support software, which runs on PCs.

**Example** The following example analyzes the failure data which was obtained from reliability tests. Values in parentheses indicate that the test equipment was shut off during the test. Failures all occurred in the same mode.

(25), 36, 50, (85), 121, 135, 161, (187), 201, 258
Table B-2. Worksheet

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Order i</th>
<th>Reverse Order (N_i = n - i + 1)</th>
<th>Failure Period Data</th>
<th>Failure Mode Mj</th>
<th>Hazard Value (h_i = 1/N_i)</th>
<th>Cumulative Hazard Value (H_i)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>25</td>
<td>–</td>
<td>0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>9</td>
<td>36</td>
<td>X</td>
<td>0.111</td>
<td>0.111</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>8</td>
<td>50</td>
<td>X</td>
<td>0.125</td>
<td>0.236</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>85</td>
<td>–</td>
<td>0.142</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>121</td>
<td>X</td>
<td>0.166</td>
<td>0.402</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>135</td>
<td>X</td>
<td>0.2</td>
<td>0.602</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>4</td>
<td>161</td>
<td>X</td>
<td>0.25</td>
<td>0.852</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>187</td>
<td>–</td>
<td>0.333</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>201</td>
<td>X</td>
<td>0.5</td>
<td>1.352</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>258</td>
<td>X</td>
<td>1</td>
<td>2.352</td>
<td></td>
</tr>
</tbody>
</table>

Figure B-4. Probability Paper
### APPENDIX C ACCELERATED MODEL EXPRESSIONS FOR TEMPERATURE/HUMIDITY TESTS

<table>
<thead>
<tr>
<th>No.</th>
<th>Presented by</th>
<th>Model Expression</th>
<th>Other</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Koyama et al.</td>
<td>$A = \exp (\alpha \cdot RH)$</td>
<td>$A$: Acceleration rate $\alpha = -0.12$</td>
</tr>
<tr>
<td>2</td>
<td>Itobayasi et al.</td>
<td>$\ln (TTF) = \ln P$</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Sinnadurai</td>
<td>$t = P^{-1}$</td>
<td>$t$: time before reaching 10% of cumulative failures</td>
</tr>
<tr>
<td>4</td>
<td>Reich et al.</td>
<td>$\lambda = \exp (A + B (T + RH))$</td>
<td>$A$, $B$: Constants</td>
</tr>
<tr>
<td>5</td>
<td>Merett et al.</td>
<td>$TTF = \exp (0.0004RH^2 + \frac{\phi}{kT})$</td>
<td>$\phi = 0.13$ to 1.5 eV</td>
</tr>
<tr>
<td>6</td>
<td>Gunn et al.</td>
<td>$R(T, RH, \phi, v) = V \cdot \exp (\frac{\phi}{kT}) \times \exp(\lambda (RH - RH_i))$</td>
<td>Left side: Median life $\lambda$: Humidity constant</td>
</tr>
<tr>
<td>7</td>
<td>Suzuki et al.</td>
<td>$Median_Life = C \cdot \exp \left( \frac{\phi}{kT} \cdot f(RH) \right)$</td>
<td>$A$: Acceleration coefficient $\phi = 1.5$ to 1.8 eV</td>
</tr>
<tr>
<td>8</td>
<td>Lycoudes et al.</td>
<td>$Median_Life = A \cdot \exp \left( \frac{\phi}{kT} \cdot \exp \left( \frac{B}{RH} \right) \cdot \frac{C}{V} \right)$</td>
<td>$A$, $B$, $C$: Constants</td>
</tr>
<tr>
<td>9</td>
<td>Maeda et al.</td>
<td>$\ln \left( \frac{L_n}{L_L} \right) = -\frac{E}{k} \left( \frac{1}{T} - \frac{1}{T_n} \right)$</td>
<td>$L_n$: Life in base mode $L_L$: Life in accelerated mode $T_n$ Constant</td>
</tr>
<tr>
<td>10</td>
<td>Peck et al.</td>
<td>$t_n = (RH)^{-n} \cdot \exp \left( \frac{E}{kT} \right)$ $R_c = (85/RH)^{-1} \cdot \left( \exp \left( 10444 \frac{1}{T} - 0.0027933 \right) \right)$</td>
<td>$n = 2.66$ to $3.0$, $E = 0.79$ to $0.90$ $R_c$: Relative life when standard is $85^\circ C$ and $85%$ RH</td>
</tr>
<tr>
<td>11</td>
<td>Setoya</td>
<td>$\Delta h_{FE} = C_1 \log t + C_2 \left( \frac{RH}{10^5} \times \exp \left( \frac{C_3}{T} \right) \right)$ $t = A \cdot P^n$</td>
<td>$C_1$ to $C_5$: Constants $t$: Test period corresponds to 10 years of $T = 35^\circ C$ and $RH = 85%$ $A = 8.76E4$ $n = -2.05$</td>
</tr>
<tr>
<td>12</td>
<td>Tanimoto</td>
<td>$L_{50} = A \cdot \exp \left( \frac{\phi}{kT} \right) \cdot \exp (-\beta \cdot RH)$</td>
<td>$L_{50}$: Half-brightness period for LED $\phi = 0.8342$ $A = 3.261E-11$ $\beta = 9.804E-4$</td>
</tr>
</tbody>
</table>

TTF: Failure period, $k$: Boltzmann’s constant, $\lambda$: Failure rate, $T$: Absolute temperature, $\phi$, $E$: Activation energy, $V$: Applied voltage, $P$: Steam pressure

**Reference**
- K.Takahisa et al. *“Device and Component Reliability Testing,”* Union of Japanese Scientists and Engineers
APPENDIX D  Q & A

The following are questions and answers concerning Compound Semiconductor Devices Division's semiconductor products.

D.1 General Q & A

Q1. What is the defect mixing rate?
   At that time, how much ppm is the defect rate?
A1. Compound Semiconductor Devices Division checks all its products before shipment. Basically, therefore, 100% of the delivered products are non-defective.
   Although the probability is low, however, even a product that was judged to be non-defective when it is shipped may have a potential problem and this problem may surface when thermal stress is applied to the product when it is mounted. The defect mixing rate naturally varies depending on the device but is 100 ppm at most.
   This rate excludes the failures (such as electrostatic breakdown or bent leads) that may occur when the product is handled by the customer, or defects that occur because of differences between the product characteristic specifications and the specifications requested by the customer.

Q2. What are the operating temperature ranges of Tr and Di?
   (The data sheet shows "storage temperature range" but does not show the operating temperature range.)
A2. Ambient temperature is defined for ICs because ICs do not function if the ambient temperature exceeds the maximum rating. However, the temperature range of Tr and Di differs depending on how they are used (depending on the applied current and voltage). Therefore, Tj is defined for Tr and Di. For the operating temperature range, refer to the relationship between Pt (W) and Ta or Tc (derating).
   (Supplement)
   The maximum value of Pt defined as the maximum rating drops with temperature if room temperature, defined as 25°C, is exceeded. When Ta reaches 150°C, Pt (W) is 0.
   This means that no current flows at 150°C.

D.2 Q & A concerning failure rate

D.2.1 General questions concerning failure rate

Q3. Do semiconductor products of standard quality grade and special quality grade differ in failure rate (Fit)?
A3. The failure rate of a product of standard quality grade and that of a product of special quality grade (A), for which screening is reinforced, is identical.
   (Supplement)
   The failure rate changes over time after product use starts. Because there is a certain probability of potential semiconductor product failure, the failure rate is relatively high when use of the products is started, but decreases over time to a certain level.
   The failure rate defined to the customer is this certain level of failure rate (equivalent to the random failure stage of bathtub curve). This failure rate is mainly determined by product design and has nothing to do with reinforcement of screening.
Q4. Is it possible to estimate the life expectancy from the failure rate?
A4. No. The failure rate indicates the probability of failure per unit time as explained in 2.1.2, and the life expectancy is the life itself of one product.

Q5. How long is the life expectancy of a semiconductor device?
A5. The actual life expectancy of a semiconductor device is determined by the durability of the elements making up the device, such as wiring, oxide film, and transistors. The durability of these elements in a semiconductor device is determined by reliability design (see 1.2.3). The life expectancy of a device of standard quality grade, for example, is designed to be at least 10 years if the device is used within the recommended operating conditions.

Q6. Can the failure rate (FIT) be converted into MTBF*?
A6. MTBF is expressed by the reverse number of the total of the failure rates of each product used in a customer’s set. Compound Semiconductor Devices Division defines the failure rate of a product. If the failure rates of the other components are known, MTBF can be calculated by the customer.

* Mean Time Between Failures

Q7. (fit) is used as the failure rate unit. Can this be converted into defect rate (ppm)?
A7. The failure rate (FIT) cannot be simply converted into defect rate (ppm). See 2.1.2.

Q8. Is the failure rate a guaranteed value (rated value)?
A8. The failure rate of a semiconductor device defined by Compound Semiconductor Devices Division is an expected value and not a guaranteed value. The failure rate is an estimated value that is derived by statistical techniques from limited data such as the results of reliability tests and claims received from the market. According to the MIL Standard (MIL-STD-690B), close to 2,000 devices must be tested to prove 10 (FIT) at a reliability standard of 60% (if an accelerated test is conducted for 1,000 hours at an acceleration coefficient of 50), which is not practical.

D.2.2 Calculating failure rate

Q9. What is the meaning of temperature parameter $\pi T$?
A9. Semiconductor devices are very sensitive to thermal stress. Thermal stress is determined by the ambient temperature at the place where the device is used, and the power supplied to the device when it is used. Generally, these two parameters vary depending on the operating conditions of the device. Temperature stress acceleration $\pi T$ is defined so that the customer can correct the failure rate. $\pi T$ is the acceleration coefficient at an actual operating temperature, where the reference temperature is 55°C.

Q10. What is the meaning of supply voltage parameter $\pi V$?
A10. The operating voltage value of active components such as transistors and diodes is determined by the customer’s design. If the components are used under conditions close to the maximum ratings, the failure rate is relatively high. If they are used well within the maximum ratings, the failure rate is low. $\pi V$ is stress acceleration by voltage. Calculate $\pi V$ for transistors. $\pi V$ is “1” for an IC.
Q11. What is the meaning of activation energy $E_a$?
A11. The energy applied from an external source to a semiconductor device until a failure occurs is called activation energy. Activation energy is derived from the result of a life test conducted under multiple stress conditions, and depends on the failure mode. Compound Semiconductor Devices Division uses 0.7 ev as a typical value if the failure mode cannot be identified.

Q12. What is the meaning of reliability standard 60%?
A12. Reliability standard means probability. The failure rate is an estimated value that is calculated by statistical technique. Reliability standard 60% means that the probability is 60%. For example, if the basic failure rate of a semiconductor device is 15 (flip), this means that the probability that the actual failure rate is within 15 (flip) is 60%, and that the probability that it exceeds 15 (flip) is 40%.

D.2.3 Question concerning storage

Q13. Notes on storing devices for long time
A13. <1> Basically, the reliability of a product is not affected in a normal storage environment ($T_A = 5$ to $30^\circ \text{C}$, RH = 20 to 70%).

<2> Dry pack products can be stored for about 2 years after manufacture without problem in the packing delivered by Compound Semiconductor Devices Division and in a normal storage environment. The point to be noted if a device is stored for a long time is wettability of the leads. If a device is stored for 2 years or longer, it is considered that worsening of wettability can be reduced by re-sealing the leads after 2 years, but testing solder wettability when using the device is recommended.

References
- Selection Guide
- Taping Specifications
- Application Note
- Data Sheet
- Reliability-related Documents

These manuals can be obtained from the Compound Semiconductor Devices Division website.
http://www.ncsd.necel.com/

(Where to find this manual)
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