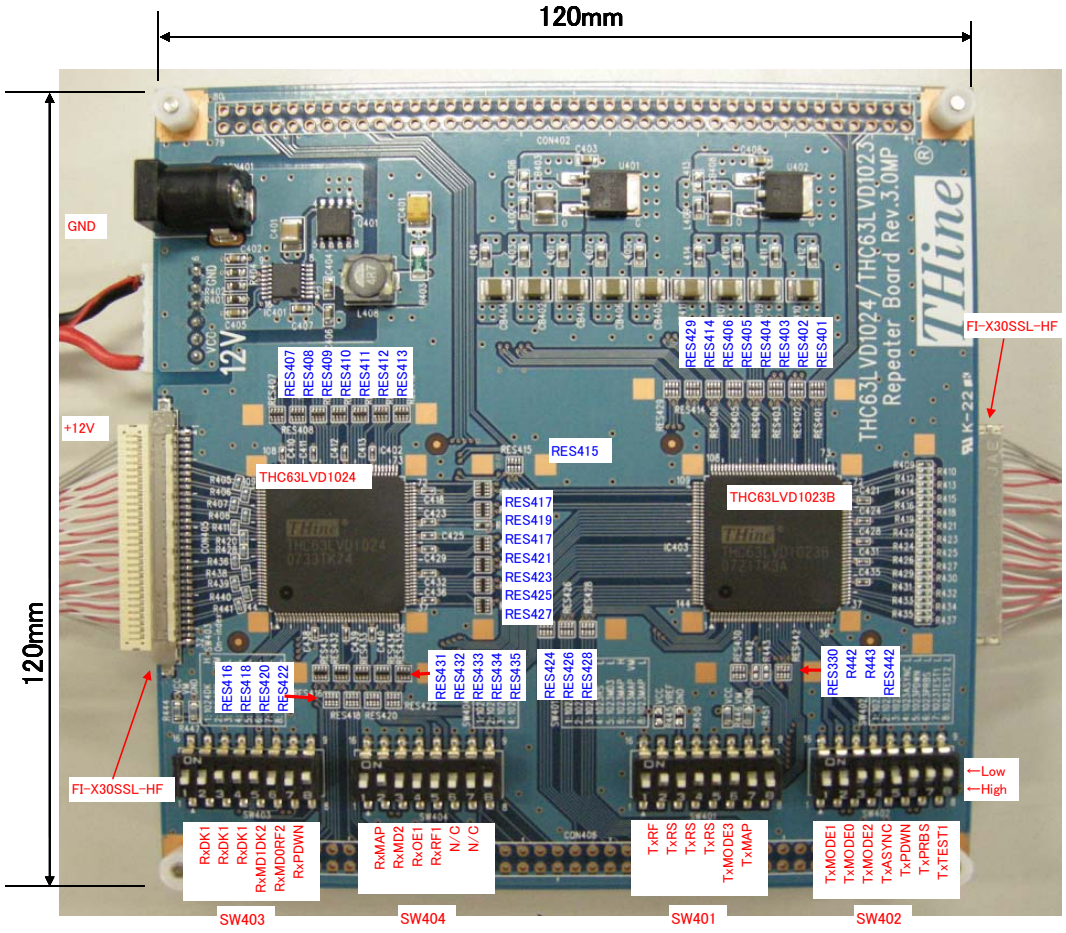
CEL California Eastern Laboratories | THine THine Electronics, Inc.
World's Leading Company in Mixed Signal Technologies

To Our Customers

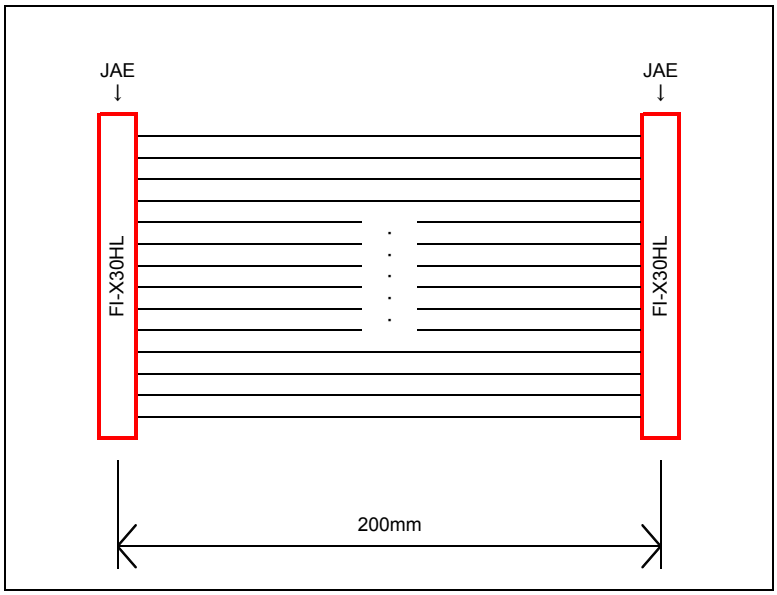
Continuing it's rich tradition of partnering with high quality Japanese semiconductor suppliers, CEL is now partnering with THine from May of 2015 onwards.

Description

t=1.6mm



LVDS-Cable Type.



SW401 Setting

* Def. : Default Setting

SW Pin#	* Def.	NodeName	THC63LVD1023B IC Pin#	PinName	Description
1	H	TxRF	21	R/F	Input Clock Triggering Edge Select. H : Rising edge, L : Falling edge
2	L	TxRS	22	RS	LVDS swing mode, VREF select.
3	H				
4	H				
5	L	TxMODE3	23	MODE3	Input port switching function enable when MODE<1:0>=HL(Single-in/Dual-out Mode). H or Open: Port switch disable. L: Port switch enable.
6	L	TxMAP	24	MAP	LVDS mapping table select.
7	H				
8	H				

SW-Pin# 2	SW-Pin# 3	SW-Pin# 4	RS	LVDS Swing	Small Swing Input Support
L	H(open)	H(open)	VIHM	350mV	N/A
H(open)	L	H(open)	VIMM	350mV	RS=VREFa
H(open)	H(open)	L	VILM	200mV	N/A

a) VREF is Input Reference Voltage.

SW-Pin# 6	SW-Pin# 7	SW-Pin# 8	RS	Mapping Mode
L	H(open)	H(open)	VIHM	Mapping MODE1
H(open)	L	H(open)	VIMM	Mapping MODE2
H(open)	H(open)	L	VILM	Mapping MODE3

SW402 Setting

* Def. : Default Setting

SW Pin#	* Def.	NodeName	THC63LVD1023B IC Pin#	PinName	Description
1	H	TxMODE1	25	MODE1	Pixel Data Mode.
2	H	TxMODE0	26	MODE0	
3	L	TxMODE2	27	MODE2	The use of these multi-function depends on the setting of MODE<1:0> or ASYNC. ASYNC=H(MODE<1:0>=Don't care.) H: Cross point switching enable. L: Cross point switching disable. ASYNC=L MODE<1:0>=HH(Single-in/Single-out Mode) H: Distribution function enable. L: Distribution function disable. MODE<1:0>=HL(Single-in/Dual-out Mode) H: DDR (Double Edge input) function enable. L: DDR (Double Edge input) function disable.
4	L	TxASYNC	28	ASYNC	Asynchronous function enable. H : Asynchronous mode enable.(MODE<1:0>=Disable) L : Asynchronous mode disable.(MODE<1:0>=Enable)
5	H	TxPDWN	30	/PDWN	H: Normal operation, L: Power down (all outputs are Hi-Z)
6	L	TxPRBS	31	PRBS	PRBS(Pseudo-Random Binary Sequence) generator is active in order to evaluate eye patterns when MODE<1:0> = LL(Dual-in/Dual-out mode) or ASYNC=H H: PRBS generator is enable. L: Normal Operation
7	L	TxTEST1	32	Reserved	Must be tied to GND.
8	H	TxTEST2	33	N/C	Must be Open.

MODE1	MODE0	Mode
H	H	Single Link(Single-in/Single-out)
H	L	Single Link(Single-in/Dual-out)
L	H	Dual Link(Dual-in/Single-out)
L	L	Dual Link(Dual-in/Single-out)

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SW403 Setting

* Def. : Default Setting

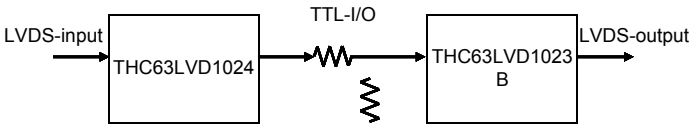
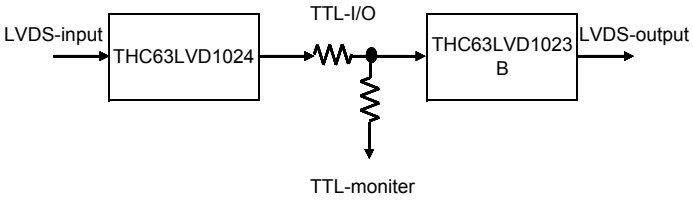
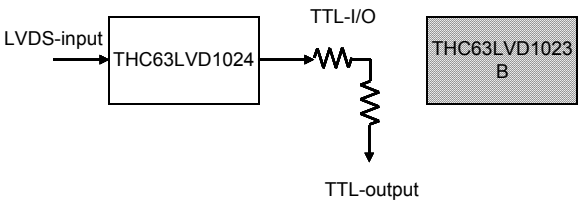
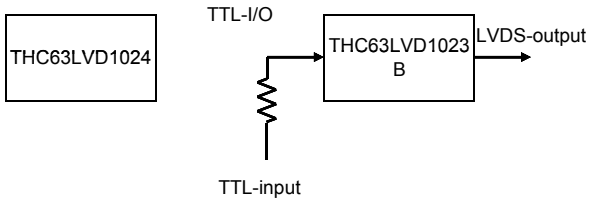
<table>
<tr><th rowspan="2">SW Pin#</th><th rowspan="2">* Def.</th><th rowspan="2">NodeName</th><th colspan="3">THC63LVD1024</th></tr>
<tr><th>IC Pin#</th><th>PinName</th><th>Description</th></tr>
<tr><td>1
2
3</td><td>H
H
L</td><td>RxDK1</td><td>7</td><td>DK</td><td>Output Clock Delay Timing Select.
tDOUT=Output Data Cycle
<table>
<tr><th rowspan="2">MODE[1:0]</th><th colspan="3">SW-Pin#</th><th rowspan="2">Offset[nsec]</th></tr>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td rowspan="3">LL
HH
HL</td><td>L</td><td>H(open)</td><td>H(open)</td><td>$6\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>L</td><td>H(open)</td><td>$-6\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>H(open)</td><td>L</td><td>0</td></tr>
<tr><td rowspan="3">LH</td><td>L</td><td>H(open)</td><td>H(open)</td><td>$7\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>L</td><td>H(open)</td><td>$-7\frac{tDOUT}{28}$</td></tr>
<tr><td>H(open)</td><td>H(open)</td><td>L</td><td>0</td></tr>
</table></td></tr>
<tr><td>4
5</td><td>L
L</td><td>RxMD1DK2
RxMD0RF2</td><td>6
5</td><td>MODE1
MODE0</td><td>Pixel Data Mode.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>H</td><td>H</td><td>Single Link(Single-in/Single-out)</td></tr>
<tr><td>H</td><td>L</td><td>Single Link(Single-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Dual Link(Dual-in/Single-out)</td></tr>
<tr><td>L</td><td>L</td><td>Dual Link(Dual-in/Single-out)</td></tr>
</table></td></tr>
<tr><td>6</td><td>H</td><td>RxPDWN</td><td>4</td><td>/PDWN</td><td>Power down and Output Control.
H : Normal operation
L : Power down</td></tr>
<tr><td>7</td><td>H</td><td>RxOE2</td><td>3</td><td>Reserved</td><td>Must be tied to VCC.</td></tr>
<tr><td>8</td><td>L</td><td>RxTEST</td><td>144</td><td>LGND</td><td>Ground Pins for LVDS inputs.</td></tr>
</table>

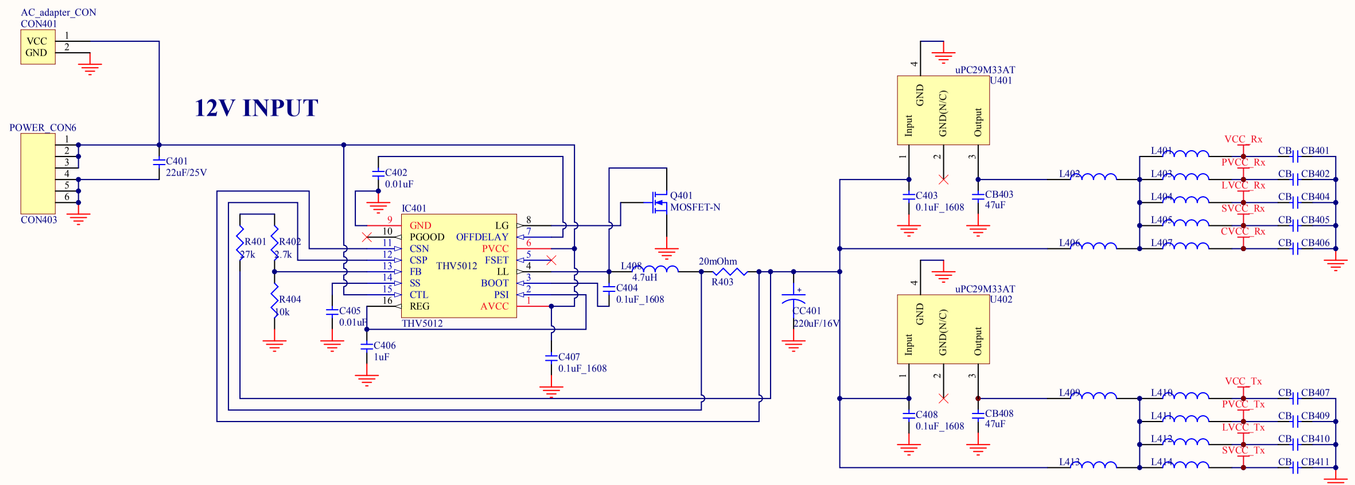
SW404 Setting

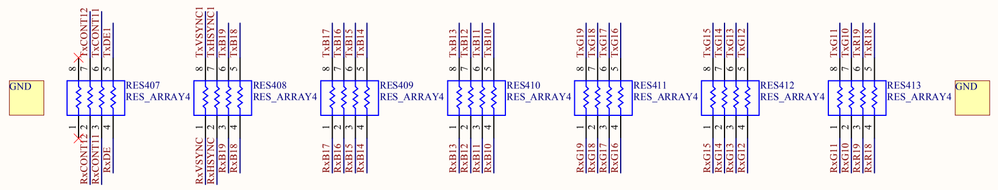
* Def. : Default Setting

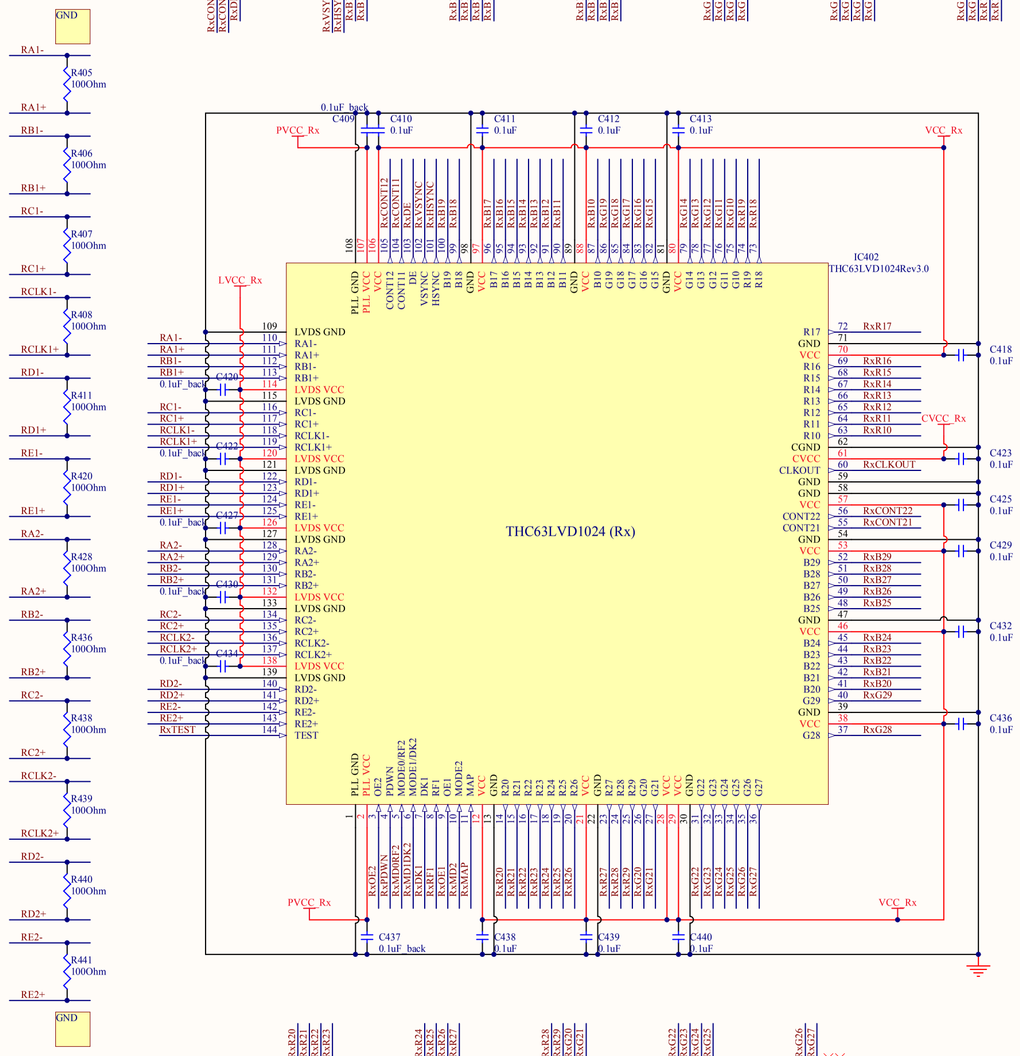
<table>
<tr><th rowspan="2">SW Pin#</th><th rowspan="2">* Def.</th><th rowspan="2">NodeName</th><th colspan="3">THC63LVD1024</th></tr>
<tr><th>IC Pin#</th><th>PinName</th><th>Description</th></tr>
<tr><td>1</td><td>H</td><td>RxMAP</td><td>11</td><td>MAP</td><td>LVDS mapping table select.
H : Mapping Mode1
L : Mapping Mode2</td></tr>
<tr><td>2</td><td>L</td><td>RxMD2</td><td>10</td><td>MODE2</td><td>DDR function enable.
<table>
<tr><th>MODE<1:0></th><th>MODE2</th><th>Mode</th></tr>
<tr><td rowspan="2">LH</td><td>H</td><td>DDR (Double Edge Output) function enable.</td></tr>
<tr><td>L</td><td>DDR (Double Edge Output) function disable.</td></tr>
<tr><td>LL
HL
HH</td><td>L</td><td>Must be tied to GND</td></tr>
</table></td></tr>
<tr><td>3</td><td>H</td><td>RxOE1</td><td>9</td><td>OE</td><td>Output Enable.
H : Output enable,
L : Output disable</td></tr>
<tr><td>4</td><td>H</td><td>RxRF1</td><td>8</td><td>R/F</td><td>Output Clock Triggering Edge Select.
H : Rising edge.
L : Falling edge.</td></tr>
<tr><td>5</td><td>H</td><td>N/C</td><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">Non Connected</td></tr>
<tr><td>6</td><td>H</td><td>N/C</td></tr>
<tr><td>7</td><td>H</td><td>N/C</td></tr>
<tr><td>8</td><td>H</td><td>N/C</td></tr>
</table>

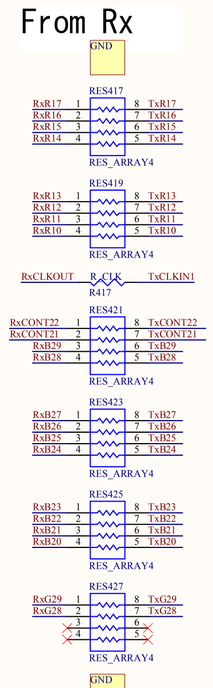
Measures Type

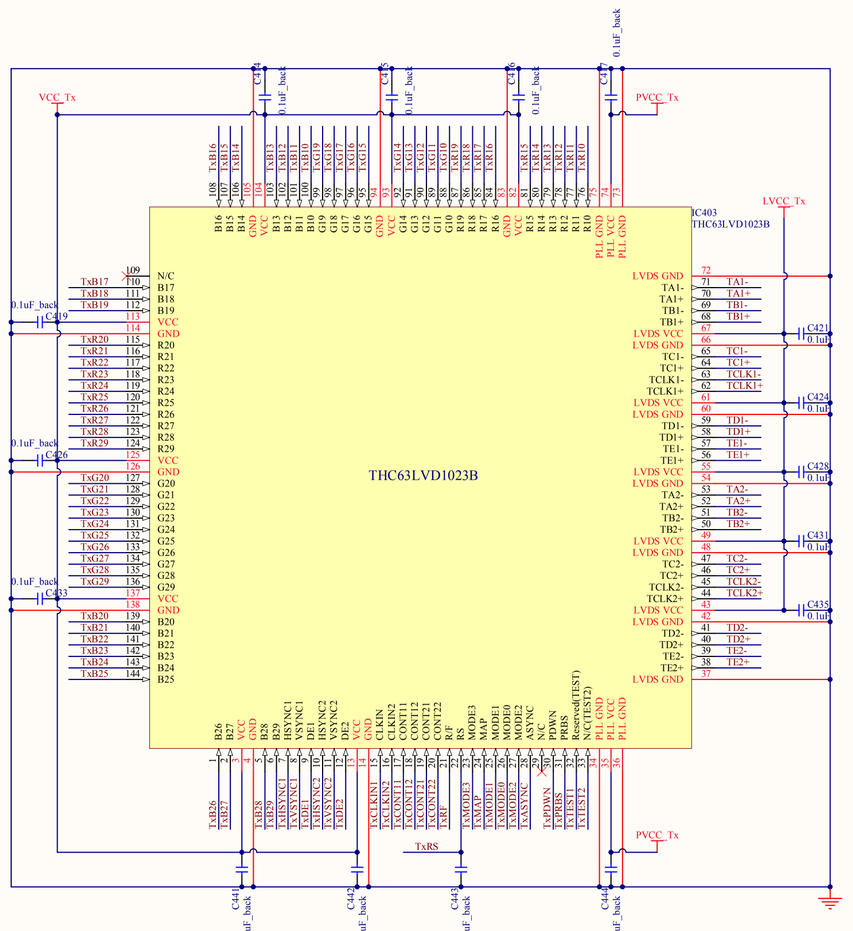
#	Type	Un-Mount	0Ω-Mount	33Ω-Mount
1		RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 **RES418 R443**		RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 **RES421**
2			RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 RES418 R443	RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 RES421
3		THC63LVD1023B	RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 RES418 R443	RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 RES421
4		RES407 RES423 RES408 RES425 RES409 RES427 RES410 RES431 RES411 RES432 RES412 RES433 RES413 RES434 RES417 RES435 RES419 R417 RES421	RES401 RES420 RES402 RES422 RES403 RES424 RES404 RES426 RES405 RES428 RES406 RES429 RES414 RES430 RES415 RES442 RES416 R442 RES418 R443	

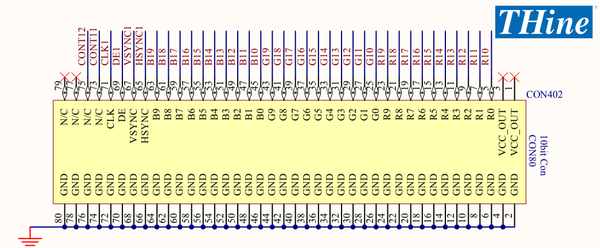


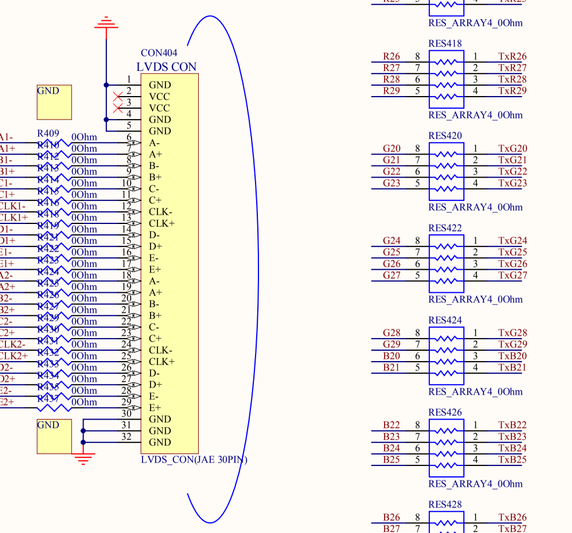


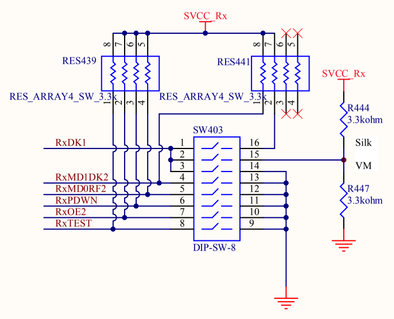


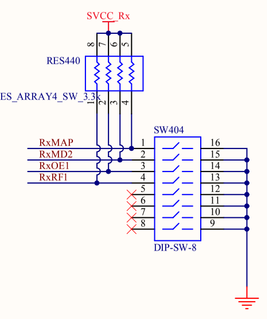


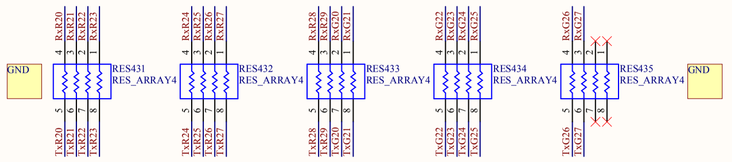


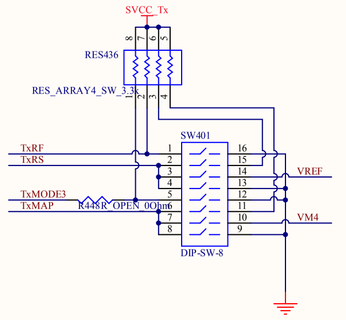


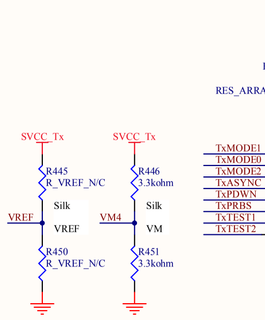


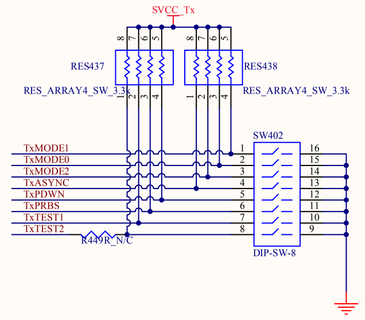


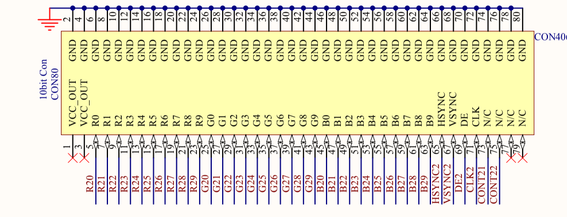












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THC63LVD1024 -> THC63LVD1023 (Repeater Board)

Title	THC63LVD1024/TH63LVD1023 Repeater Board Rev3.0MP		
Size	Number		Revision
A1			
Date:	2007/11/29	Sheet of	
File:	C:\rain\...\1024-1023B_rev3mp_E.SCHDOC	Drawn By:	Rei Fujiki

Comment	Designator	Description	Package	Manufacturer	Quantity
22uF/25V	C401	Capacitor	SMT3225		1
0.01uF	C402, C405	Capacitor	SMT1608		2
0.1uF_1608	C403, C404, C407, C408	Capacitor	SMT1608		4
1uF	C406	Capacitor	SMT1608		1
0.1uF_back	C409, C414, C415, C416, C417, C419, C420, C422, C426, C427, C430, C433, C434, C437, C441, C442, C443, C444	Capacitor	SMT1608		18
0.1uF	C410, C411, C412, C413, C418, C421, C423, C424, C425, C428, C429, C431, C432, C435, C436, C438, C439, C440	Capacitor	SMT0603		18
CB	CB401, CB402, CB404, CB405, CB406, CB407, CB409, CB410, CB411	GRM32EB11A106KC01	SMT3225	murata	9
47uF	CB403, CB408	Capacitor	SMT3225		2
220uF/16V	CC401	T520B157M006ATE045	SMT3528	KEMET	1
AC_adapter_CON	CON401	MJ-179P	DC Jack : Mating Plug 5.5x2.1	Marushin	1
CON80	CON402, CON406	2x40 Pin Header	2.54mm pitch (2x40pin)		2
POWER_CON6	CON403	S 6B-EH	2.5mmpitch 6pin	JST	1
LVDS_CON(JAE 30PIN	CON404, CON405	FI-X30SSL-HF	FI-X30SSL-HF	JAE	2
THV5012	IC401	THV5012	TSSOP16 Pins	THine	1
THC63LVD1024	IC402	THC63LVD1024	LQFP 144pin Exposed PAD	THine	1
THC63LVD1023B	IC403	THC63LVD1023B	LQFP 144pin	THine	1
L	L401, L402, L403, L404, L405, L406, L407, L409, L410, L411, L412, L413, L414	MPZ1608B471A	SMT1608	TDK	13
4.7uH	L408	RLF7030T-4R7M3R4	RLF Series	TDK	1
MOSFET-N	Q401	uPA2706	Power HSOP8	NEC	1
27k	R401	Resistance	SMT1608		1
2.7k	R402	Resistance	SMT1608		1
20mOhm	R403	RL1632T-R015-G	SMT3216	Susumu	1
10k	R404	Resistance	SMT1608		1
100Ohm	R405, R406, R407, R408, R411, R420, R428, R436, R438, R439, R440, R441	Resistor	SMT1005		12
0Ohm	R409, R410, R412, R413, R414, R415, R416, R418, R419, R421, R422, R423, R424, R425, R426, R427, R429, R430, R431, R432, R433, R434, R435, R437	Resistor	SMT1005		24
R_CLK	R417	Resistor 33ohm	SMT1005		1
R_CLK_0Ohm	R442, R443	Resistor	SMT1005		2
3.3kohm	R444, R446, R447, R451	Resistance	SMT1608		4
R_VREF_N/C	R445, R450	Resistance	SMT1608		2
R_OPEN_0Ohm	R448	Resistance	SMT1608		1
R_N/C	R449	Resistance	SMT1608		1
RES_ARRAY4_0Ohm	RES401, RES402, RES403, RES404, RES405, RES406, RES414, RES415, RES416, RES418, RES420, RES422, RES424, RES426, RES428, RES429, RES430, RES442	Resistor Array	SMT 2010		18
RES_ARRAY4	RES407, RES408, RES409, RES410, RES411, RES412, RES413, RES417, RES419, RES421, RES423, RES425, RES427, RES431, RES432, RES433, RES434, RES435	Resistor Array 33ohm	SMT 2010		18
RES_ARRAY4_SW_3.3k	RES436, RES437, RES438, RES439, RES440, RES441	Resistor Array	SMT 2010		6
DIP-SW-8	SW401, SW402, SW403, SW404	A6S-8104	A6S-8104	omron	4
uPC29M33AT	U401, U402	uPC2933AT-AZ	SC-63	NEC	2

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Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them
3. This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
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5. This product is presumed to be used for general electric equipment, not for the applications which require very hi reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear contro equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applyi appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have suffici redundant or error preventive design applied to the use of the product so as not to have our product cause any soc or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic good under the Foreign Exchange and Foreign Trade Control Law.

THine Electronics, Inc.

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