THCX423R10

High Performance Bi-directional Active Switch with Equalizer

General Description

The THCX423R10 is a high performance bi-directional active switch for USB3.1 Gen1 and high speed interface like V-by-One® HS.

The THCX423R10 features a continuous time linear equalizer (CTLE) to provide a boost up to +11.6dB at 5 GHz. It opens an input eye even though it is completely closed due to inter-symbol interference (ISI) induced by the inter-connect mediums. The transmitter features a programmable output de-emphasis driver with up to -8.5 dB and allows adjustable amplitude voltage from 600mVp-p to 1300mVp-p to suit multiple application scenarios.

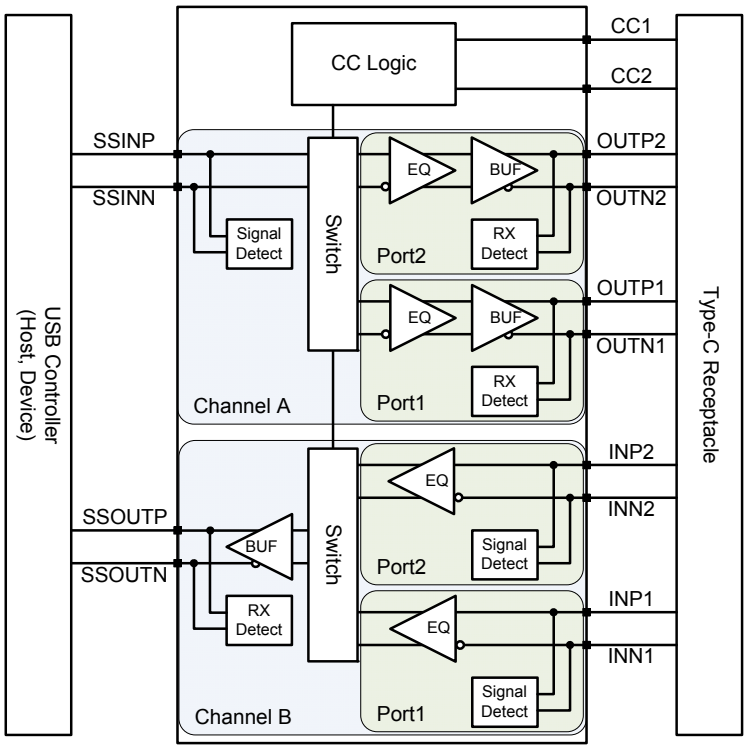
Features

- MUX and DEMUX
- Receive Equalization up to +11.6dB@5GHz
- Transmit De-Emphasis up to -8.5dB
- Transmit VOD Control : 600 to 1300 mVp-p
- Support USB 3.1 Gen1 and USB Type-C™
  - Integrated CC Logic
  - Receiver and LFPS Detect
- Available in single supply voltage 3.3V with integrated LDO
- ESD: HBM ±4kV
- QFN40 (5.0mm x 5.0mm)

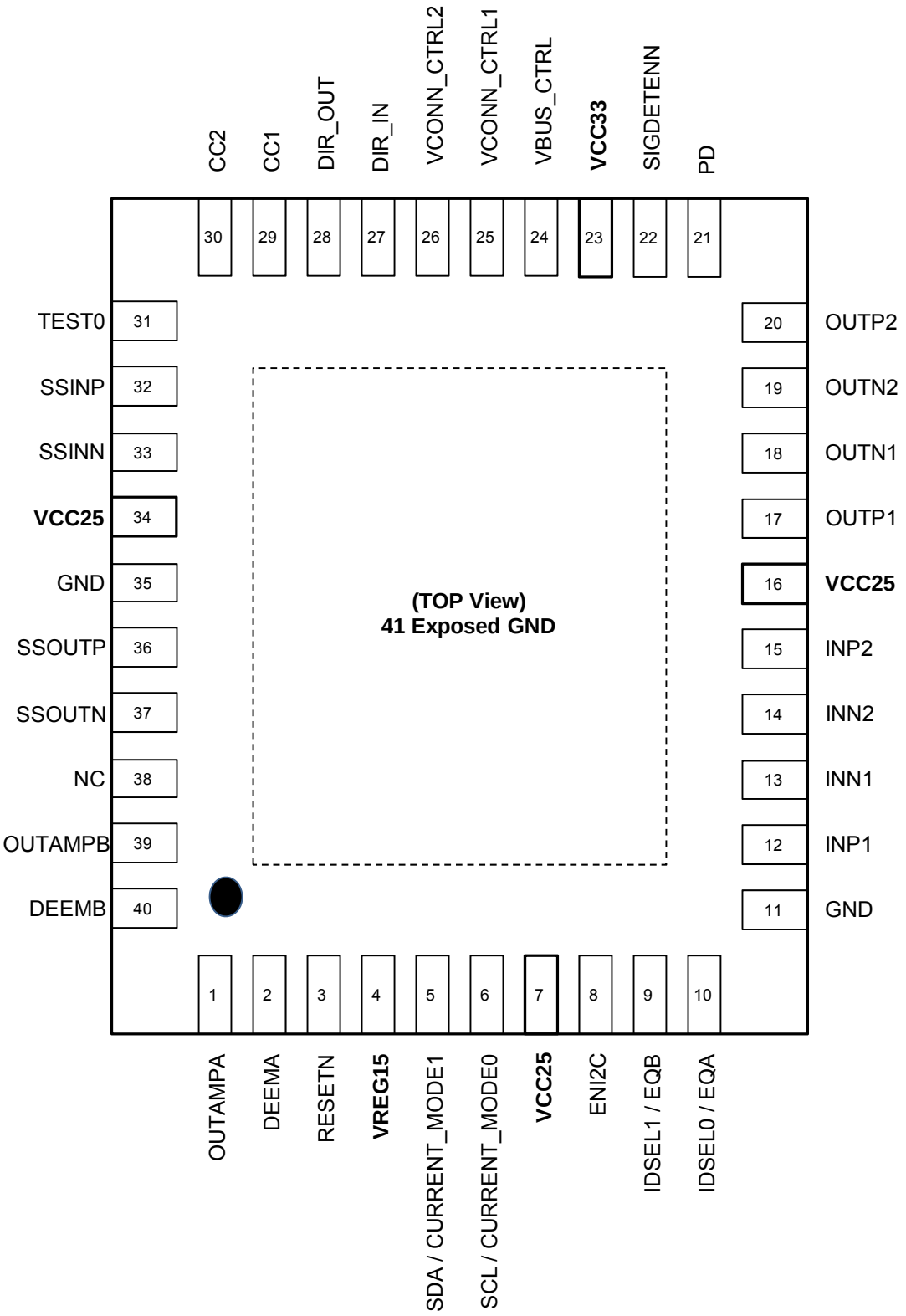
Applications

- Flip-ability USB Type-C™
- USB Host and Devices
- V-by-One® HS
- CML Interface

Block Diagram



Pin Configuration



Pin Description

Pin Name	Pin No	Type	Description
SSINP	32	CI	Super-Speed CML Channel A (CHA) Signal Input (USB controller side)
SSINN	33	CI	Super-Speed CML Channel A (CHA) Signal Input (USB controller side)
SSOUTP	36	CO	Super-Speed CML Channel B (CHB) Signal Output (USB controller side)
SSOUTN	37	CO	Super-Speed CML Channel B (CHB) Signal Output (USB controller side)
OUTP1	17	CO	Super-Speed CML Port 1 of CHA Signal Output (Type-C Receptacle side)
OUTN1	18	CO	Super-Speed CML Port 1 of CHA Signal Output (Type-C Receptacle side)
OUTP2	20	CO	Super-Speed CML Port 2 of CHA Signal Output (Type-C Receptacle side)
OUTN2	19	CO	Super-Speed CML Port 2 of CHA Signal Output (Type-C Receptacle side)
INP1	12	CI	Super-Speed CML Port 1 of CHB Signal Input (Type-C Receptacle side)
INN1	13	CI	Super-Speed CML Port 1 of CHB Signal Input (Type-C Receptacle side)
INP2	15	CI	Super-Speed CML Port 2 of CHB Signal Input (Type-C Receptacle side)
INN2	14	CI	Super-Speed CML Port 2 of CHB Signal Input (Type-C Receptacle side)
PD	21	I	Power Down 0: Operation 1: Chip Power Down
SIGDETENN	22	I	Signal Detect Enable 0: Enable 1: Disable
TEST0	31	I	Test pin. Must be tied to ground for normal operation.
RESETN	3	I	Reset 0:Chip Reset 1:Operation
CC1	29	LCI	Type-C configuration channel signal 1
CC2	30	LCI	Type-C configuration channel signal 2
DIR_IN	27	I	Port select input 0:Port1 1:Port2
DIR_OUT	28	O	Determination result by CC Logic L:Port1 H:Port2
VCONN_CTRL1	25	O	VCONN port control signal 1 L:Not apply VCONN H:Apply VCONN
VCONN_CTRL2	26	O	VCONN port control signal 2 L:Not apply VCONN H:Apply VCONN
VBUS_CTRL	24	O	VBUS port control signal L:Not apply VBUS H:Apply VBUS

ENI2C	8	I	2-wire serial I/F enable 0:2-wire serial I/F access disable 1:2-wire serial I/F access enable
SDA/ CURRENT_MODE1	5	BO	SDA/CURRENT_MODE1 pin has dual function. SDA: SDA input /output for 2-wire serial I/F when ENI2C=1 CURRENT_MODE1: Type-C current advertisement setting when ENI2C=0
SCL/ CURRENT_MODE0	6	BO	SCL/CURRENT_MODE0 pin has dual function. SCL: SCL input for 2-wire serial I/F when ENI2C=1 CURRENT_MODE0: Type-C current advertisement setting when ENI2C=0
IDSEL0/EQA	10	3LI	IDSEL0/EQA pin has dual function. IDSEL0: 2-wire serial I/F device address setting when ENI2C=1. EQA: Controller Side Rx equalizer setting for CHA when ENI2C=0. Low:2.0dB / Float:4.0dB / High:8.0dB
DEEMA	2	3LI	Receptacle Side Tx de-emphasis setting for CHA Low:3.5dB / Float:6.0dB / High:8.5dB
OUTAMPA	1	3LI	Receptacle Side Tx output swing setting for CHA Low:600mV / Float:1000mV / High:1300mV
IDSEL1/EQB	9	3LI	IDSEL1/EQB pin has dual function. IDSEL1: 2-wire serial I/F device address setting when ENI2C=1. EQB: Receptacle side Rx equalizer setting for CHB when ENI2C=0. Low:2.0dB / Float:4.0dB / High:8.0dB
DEEMB	40	3LI	Controller side Tx de-emphasis control for CHB Low:3.5dB / Float:6.0dB / High:8.5dB
OUTAMPB	39	3LI	Controller side Tx output swing control for CHB Low:600mV / Float:1000mV / High:1300mV
VREG15	4	PWR	Decoupling capacitor pin for on-chip regulator. See Figure 1.
VCC25	7,16,34	PWR	Decoupling Capacitor Pin, 2.5V output. See Figure 1.
VCC33	23	PWR	Power supply pin for on-chip regulator. See Figure 1.
GND	11,35, 41	GND	Ground. Must be tied to the PCB ground plane through an array of vias. Pin#41 is exposed pad ground.
NC	38	NC	Non-connection pin. Must be open.

CI: CML Input buffer, CO: CML Output buffer
I: LVCMOS Input buffer, O: LVCMOS Output buffer, BO: Open-Drain LVCMOS Bi-directional
LCI: Level Control LVCMOS Input buffer, 3LI: 3-Level LVCMOS Input buffer,
PWR: Power supply, GND: Ground, NC: Non-connection pin

Functional Overview

The THCX423R10 has functions as below.

- MUX and DEMUX
- Signal Conditioning (Rx Equalizer , Tx de-emphasis, Tx output swing level)
- VBUS,VCONN port control function for USB Type-C™
- 2-wire serial I/F
- Single Supply Voltage (3.3V)

Operation Mode Settings

Table1 shows the operation mode setting.

Table 1. Operation Mode Setting

Pin Settings			Operation Mode
PD	RESETN	ENI2C	
0	0	Ignore	Chip Reset. Power Down except on-chip Regulator
	1	0	Normal Operation. Signal Conditioning Settings by External Pin
		1	Normal Operation. Signal Conditioning Settings by 2-wire serial I/F Access
1	Ignore	Ignore	Chip Power Down.

On-chip Regulator Settings

The THCX423R10 integrates the On-chip regulator for internal 2.5V and 1.5V circuit which is able to operate under the single supply voltage. On-chip regulator is turned on/off by the PD pin. Bypass VCC33 to GND with 10uF and 1uF to reduce high frequency noise. Bypass each VCC25 to GND with 0.1uF and 1uF, VREG15 to GND with 0.1uF and 1uF make stabilized and remove high frequency noise.

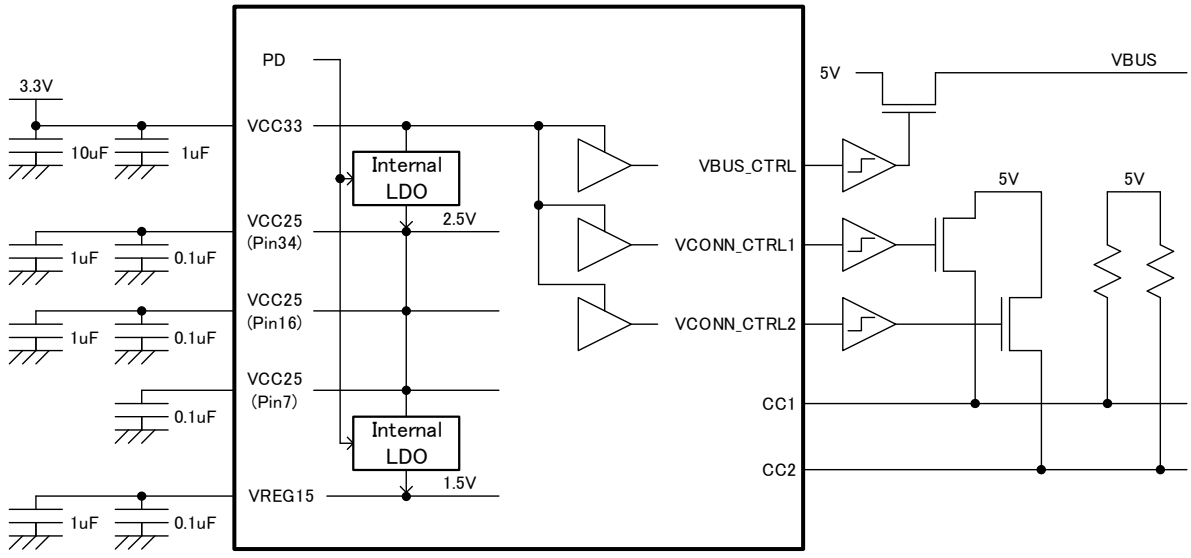


Figure 1. Connection of VCC33, VCC25, VREG15 and Decoupling Capacitor

Rx Equalization Setting

THCX423R10 receiver have controls for receiver equalization. The receiver equalization gain value can be controlled either through 2-wire serial interface registers or through pins.

Table 2. Rx Equalization Setting

Pins	Registers								@2.5GHz [dB]	@5GHz [dB]
EQx	CHx_PORT1_EQ_SET				CHx_PORT2_EQ_SET					
	7	6	5	4	3	2	1	0		
-	0	0	*	*	0	0	*	*	0	0.05
	0	1	0	*	0	1	0	*	0	0.1
	0	1	1	0	0	1	1	0	0	0.2
	0	1	1	1	0	1	1	1	0	0.3
	1	0	0	0	1	0	0	0	0	0.9
	1	0	0	1	1	0	0	1	0	1.5
0	1	0	1	0	1	0	1	0	0	2.0
-	1	0	1	1	1	0	1	1	1.3	3.8
F	1	1	0	0	1	1	0	0	1.5	4.0
1	1	1	0	1	1	1	0	1	5.1	8.0
-	1	1	1	*	1	1	1	*	8.6	11.6

x=A,B

Tx Equalization Setting

THCX423R10 transmitter have controls for de-emphasis function. The de-emphasis gain value can be controlled either through 2-wire serial registers or through pins.

De-emphasis function works under less 5ns width pulse.

Table 3. De-Emphasis Setting (CHA)

Pins	Registers						Value [dB]
DEEMA	CHA_PORT1_DEEM_SET			CHA_PORT2_DEEM_SET			
	5	4	3	2	1	0	
-	0	0	0	0	0	0	0
0	0	0	1	0	0	1	3.5
F	0	1	1	0	1	1	6.0
1	1	1	1	1	1	1	8.5

Table 4. De-Emphasis Setting (CHB)

Pins	Registers			Value [dB]
DEEMB	CHB_DEEM_SET			
	2	1	0	
-	0	0	0	0
0	0	0	1	3.5
F	0	1	1	6.0
1	1	1	1	8.5

Tx Output Swing Setting

THCX423R10 transmitter have controls for output swing amplitude. The output swing amplitude can be controlled either through 2-wire serial interface registers or through pins.

Table 5. Output Swing Setting (CHA)

Pins	Registers						Value [mVpp]
DEEMA	CHA_PORT1_VOD_SET			CHA_PORT2_VOD_SET			
	5	4	3	2	1	0	
-	0	0	0	0	0	0	-
0	0	0	1	0	0	1	600
F	0	1	1	0	1	1	1000
1	1	1	1	1	1	1	1300

Table 6. Output Swing Setting (CHB)

Pins	Registers			Value [mVpp]
DEEMB	CHB_VOD_SET			
	5	4	3	
-	0	0	0	-
0	0	0	1	600
F	0	1	1	1000
1	1	1	1	1300

Rx Detect

THCX423R10 has Receiver Detect functionality for USB3.x transmission.

Receiver Detect functionality must be disable when it is not USB3.x application.

The way to force Receiver Detect functionality output by resistor is below.

When CHA_RXDET_CTRL_EN and CHB_RXDET_CTRL_EN is 1, Receiver Detect functionality output is forced.

Table 7. Rx Detect Settings

Registers	Address	Enable (Default)	Disable
CHA_RXDET_CTRL_EN	0x09[0]	0	1
CHA_PORT1_RXDET	0x0A[1]	Don't Care	1
CHA_PORT2_RXDET	0x0A[0]	Don't Care	1
CHB_RXDET_CTRL_EN	0x0D[0]	0	1
CHB_RXDET	0x0E[0]	Don't Care	1

Signal Detect

THCX423R10 has Signal Detect functionality.

If this function is enable, the power consumption is low when signal does not input to THCX423R10.

CC Logic

THCX423R10 has function for Configuration Chanel (CC) of USB Type-C™ as below.

- Attach / Detach Detection
- Plug Orientation / Cable Twist Detection
- Configure VCONN

The following table shows how to control CC logic with ENI2C.

Table 8. 2-Wire Signal Interface Control

Settings			Control	
ENI2C	Register		VCONN_CTRL1/2, VBUS_CTRL,DIR_OUT	Port position
	OVERRIDE_CC	OVERRIDE_LANE_PD		
0	Ignore	Ignore	Pin Control (*1)	Pin Control (*2)
1	0	0	Pin Control (*1)	Pin Control (*2)
	0	1	Pin Control (*1)	Register Control (*4)
	1	0	Register Control (*3)	Pin Control (*2)
	1	1	Register Control (*3)	Register Control (*4)

*1 Controlled by CC1 and CC2 pin
*2 Controlled by DIR_IN pin
*3 Controlled by VBUS_CTRL, VCONN_CTRL1 and VCONN_CTRL2 register
*4 Controlled by pdn_CHA[1:0] and pdn_CHB[1:0] register

The Way to be disable CC logic by register is below.

Table 9. CC logic Setting

Registers	Address	Enable (Default)	Disable
OVERRIDE_CC	0x00[0]	0	1
ATTACH	0x03[4]	0	1

CC Logic(2-wire serial interface Disable)

DIR_OUT, VBUS_CTRL and VCONN_CTRL1/2 are controlled in accordance with the state of CC1 and CC2 pin as shown in the following table. ATTACH is an internal signal inside THCX423R10.

Table 10. CC Control

Case No.	CC1	CC2	DIR_OUT(*1)	VBUS_CTRL(*2)	VCONN_CTRL1(*2)	VCONN_CTRL2(*2)	ATTACH (internal signal)	Function
1	vOpen	vOpen	0	0	0	0	0	Detach. Analog/Digital Power Down
2	vRd	vOpen	0	1	0	0	1	CC1 Attach, Port1 Active
3	vOpen	vRd	1	1	0	0	1	CC2 Attach, Port2 Active
4	vOpen	vRa	0	0	0	0	0	Detach. Analog/Digital Power Down
5	vRa	vOpen	0	0	0	0	0	Detach. Analog/Digital Power Down
6	vRd	vRa	0	1	0	1	1	CC1 Attach, Port1 Active
7	vRa	vRd	1	1	1	0	1	CC2 Attach, Port2 Active
8	vRd	vRd	0	0	0	0	0	(Debug)
9	vRa	vRa	0	0	0	0	0	(Audio)

*1 0:Port1 Active, 1:Port2 Active
*2 0:Disable, 1:Enable

CC1 and CC2 pin have 3-level input IO to distinguish the voltage level of vOpen, vRd and vRa. The combination of CURRENT_MODE1 and CURRENT_MODE0 pins adjusts the threshold voltage of 3-level input IO. (Followed by the standard of USB Type-C™, the threshold voltage of each vOpen, vRd and vRa is controlled by Type-C current advertisement independently.)

Table 11. Current Mode Setting

Setting		Current Mode	CC1,CC2 pin Input Threshold Level
CURRENT _MODE1	CURRENT _MODE0		
0	0	USB Default	See Table 17
0	1	Medium(Type-C Current 1.5A)	
1	0	High(Type-C Current 3.0A)	
1	1	Used on the Device Side.	

2-wire serial I/F

THCX423R10 has 2-wire serial I/F Slave block and a customer can control high-speed analog block setting, USB Type-C™ and related functions(VCONN port control, VBUS port control, active data lane select). When ENI2C=1, 2-wire serial I/F slave is active.

Functions of 2-wire serial I/F slave block are as below.

- Standard-mode, Fast-mode, Fast-mode Plus (~1Mbps)
- Selectable 2-wire serial I/F device address (9 address)
- Burst Access acceptable
- 2-wire serial I/F bus watch dog timer
  (After receiving 2-wire serial I/F access from a host device, if SDA or SCL is stuck for long time, internal sequence circuit is cleared automatically.)

When ENI2C=1, 2-wire serial I/F device address is selectable by IDSEL1 and IDSEL0 pins. It can select 9 device addresses. See Table 12.

Table 12. Device Address

IDSEL1	IDSEL0	2-wire serial I/F Device Address [6:0] (HEX)
Low	Low	0x0C
Low	Float	0x0D
Low	High	0x0E
Float	Low	0x0F
Float	Float	0x10
Float	High	0x11
High	Low	0x12
High	Float	0x13
High	High	0x14

Register Map

Table 13. Register Map

Address (HEX)	Bit	R/W	Default (HEX)	Register Name	Descriptions	Note
0x00	7:2	R	0x03	Reserved	-	-
	1	RW		OVERRIDE_PDN_PORT	0: Allow DIR_IN pin control. 1: Block DIR_IN pin control. Use register.	-
	0	RW		OVERRIDE_CC	0: Allow CC1, CC2 pin control. 1: Block CC1, CC2 pin control. Use register	-
0x01	7:6	RW	0x20	CURRENT_MODE	00: USB Default 01: Medium (Type-C current 1.5A) 10: High (Type-C Current 3.0A) 11: Used on Device Side.	See Table 17
	5:4	RW		CC_DEBOUNCE	tCC Debounce time adjustment 00: 50ms 01: 100ms 10: 150ms (default) 11: 300ms	-
	3:2	R		CC2_MONITOR	00: vOpen 01: vRa 10: vRd 11: Reserved	Active only OVERRIDE_CC=0. Otherwise 00 fixed.
	1:0	R		CC1_MONITOR	00: vOpen 01: vRa 10: vRd 11: Reserved	
0x02	7:4	RW	0xBA	Reserved	-	-
	3:2	RW		RXDET_TIMEOUT	Rx detect timeout value setting 00:12ms 01:13.5ms 10:15ms(Default) 11:16ms	-
	1:0	RW		PD_DEBOUNCE	tPD Debounce time adjustment 00: 5ms 01: 10ms 10: 15ms (default) 11: 30ms	-
0x03	7:5	R	0x00	Reserved	-	-
	4	RW		ATTACH	Port Attach state control	Active only OVERRIDE_CC=1 Otherwise ignored.
	3	RW		DIR_OUT	DIR_OUT control	
	2	RW		VBUS_CTRL	VBUS_CTRL control	
	1	RW		VCONN_CTRL2	VCONN_CTRL2 control	
	0	RW		VCONN_CTRL1	VCONN_CTRL1 control	
0x04	7:1	R	0x00	Reserved	-	-
	0	RW		SFT_RST	Soft Reset 1: Reset registers to default value Automatically cleared into 0 after reset action. 0 is always read.	-
0x05	7:4	R	0x00	Reserved	-	-
	3:2	RW		PDN_CHA	Channel A Power Down 00:Both Port Power Down 01:Only Port2 Active 10:Only Port1 Active 11:Forbidden	Active only OVERRIDE_PDN_PORT=1 .
	1:0	RW		PDN_CHB	Channel B Power Down 00:Both Port Power Down 01:Only Port2 Active 10:Only Port1 Active 11: Forbidden	

Table 13. Register Map(continued)

Address (HEX)	Bit	R/W	Default (HEX)	Register Name	Descriptions	Note
0x06	7:6	R	0x1B	Reserved	-	-
	5:3	RW		CHA_PORT1_VOD_SET	Output swing control for OUT1(CHA PORT1 side). 001: 600mV typ 011: 1000mV typ (default) 111: 1300 mV typ other: Forbidden settings	-
	2:0	RW		CHA_PORT2_VOD_SET	Output swing control for OUT2(CHA PORT2 side). 001: 600mV typ. 011: 1000mV typ (default) 111: 1300 mV typ other: Forbidden settings	-
0x07	7:6	R	0x09	Reserved	-	-
	5:3	RW		CHA_PORT1_DEEM_SET	Tx de-emphasis control for OUT1(CHA PORT1 side). 000: 0dB 001: 3.5 dB typ (default) 011: 6 dB typ 111: 8.5 dB typ other: Forbidden settings	-
	2:0	RW		CHA_PORT2_DEEM_SET	Tx deemphasis control for OUT2(CHA PORT2 side). 000: 0dB 001: 3.5 dB typ (default) 011: 6 dB typ 111: 8.5 dB typ other: Forbidden settings	-
0x08	7:4	RW	0xAA	CHA_PORT1_EQ_SET	CHA PORT1 Rx equalizer setting. 00**: 0.05 dB 010*: 0.1 dB 0110: 0.2 dB 0111: 0.3 dB 1000: 0.9 dB 1001: 1.5 dB 1010: 2.0 dB (default) 1011: 3.8dB 1100: 4.0 dB 1101: 8.0 dB 111*: 11.6 dB	-
	3:0	RW		CHA_PORT2_EQ_SET	CHA PORT2 Rx equalizer setting. 00**: 0.05 dB 010*: 0.1 dB 0110: 0.2 dB 0111: 0.3 dB 1000: 0.9 dB 1001: 1.5 dB 1010: 2.0 dB (default) 1011: 3.8dB 1100: 4.0 dB 1101: 8.0 dB 111*: 11.6 dB	-
0x09	7:1	R	0x00	Reserved	-	-
	0	RW		CHA_RXDET_CTRL_EN	0: CHA controlled by RXDET signal(Normal Function) 1: CHA controlled by register (Address:0x0A).	-
0x0A	7:6	R	0x20	Reserved	-	-
	5	RW		CHA_RXDET_VHYS_SET	RXDET hysteresis select(CHA Both PORT) 0: 50mV 1: 100mV(default)	-
	4:2	R		Reserved	-	-
	1	RW		CHA_PORT1_RXDET	Rx detect output monitor and control(CHA PORT1 side) 0: No receiver termination. 1: detected receiver termination.	See Descriptions of Address 0x09
	0	RW		CHA_PORT2_RXDET	Rx detect output monitor and control(CHA PORT2 side) 0: No receiver termination. 1: detected receiver termination.	

Table 13. Register Map(continued)

Address (HEX)	Bit	R/W	Default (HEX)	Register Name	Descriptions	Note
0x0B	7:6	R	0x19	Reserved	-	-
	5:3	RW		CHB_VOD_SET	Output swing control for SSOUT(CHB) 001: 600mV typ. 011: 1000mV typ(default) 111: 1300 mV typ other : Forbidden settings	-
	2:0	RW		CHB_DEEM_SET	Tx deemphasis control for SSOUT(CHB) 000: 0dB 001: 3.5 dB typ(default) 011: 6 dB typ 111: 8.5 dB typ other : Forbidden settings	-
0x0C	7:4	RW	0xAA	CHB_PORT1_EQ_SET	CHB PORT1 Rx equalizer setting. 00**: 0.05 dB 010*: 0.1 dB 0110: 0.2 dB 0111: 0.3 dB 1000: 0.9 dB 1001: 1.5 dB 1010: 2.0 dB (default) 1011: 3.8dB 1100: 4.0 dB 1101: 8.0 dB 111*: 11.6 dB	-
	3:0	RW		CHB_PORT2_EQ_SET	CHB PORT2 Rx equalizer setting. 00**: 0.05 dB 010*: 0.1 dB 0110: 0.2 dB 0111: 0.3 dB 1000: 0.9 dB 1001: 1.5 dB 1010: 2.0 dB (default) 1011: 3.8dB 1100: 4.0 dB 1101: 8.0 dB 111*: 11.6 dB	-
0x0D	7:1	R	0x00	Reserved	-	-
	0	RW		CHB_RXDET_CTRL_EN	0: CHB controlled by RXDET signal(Normal Function) 1: CHB controlled by register (Address:0x0E).	-
0x0E	7:6	R	0x20	Reserved	-	-
	5	RW		CHB_RXDET_VHYS_SET	RXDET hysteresis select(CHB) 0: 50mV 1: 100mV(default)	-
	4:1	R		Reserved	-	-
	0	RW		CHB_RXDET	Rx detect output monitor and control(CHB) 0: No receiver termination. 1: detected receiver termination.	-
0x0F	7:1	R	0x00	Reserved	-	-
	0	RW		Reserved	-	-

Absolute Maximum Ratings

Table 14. Absolute Maximum Ratings

Parameter			Min	Typ	Max	Unit
Supply Voltage(VCC33)			-0.3	-	4.0	V
LVCMOS Input/Output Voltage			-0.3	-	VCC33+0.3	V
Open-Drain LVCMOS Bi-directional Input/Output Voltage			-0.3	-	VCC33+2.5	V
Level Control LVCMOS Input Voltage			-0.3	-	VCC33+2.5	V
3-Level LVCMOS Input Voltage			-0.3	-	VCC33+0.3	V
CML Receiver Input Voltage			-0.3	-	3.0	V
CML Transmitter Output Voltage			-0.3	-	3.0	V
ESD Rating	HBM	High-Speed CML CC1,CC2	-	-	±4	kV
		All Other Pin	-	-	±2	
	MM		-	-	±200	V
	CDM		-	-	±500	V
Storage Temperature			-55	-	125	°C
Junction Temperature			-	-	125	°C
Reflow Peak Temperature/Time			-	-	260/10	°C/sec

Recommended Operating Conditions

Table 15. Recommended Operating Condition

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC33)	3.0	3.3	3.6	V
Supply Ramp Requirement	0.1	-	50	ms
Operating Temperature	-40	-	85	°C

Equivalent CML Input Diagram

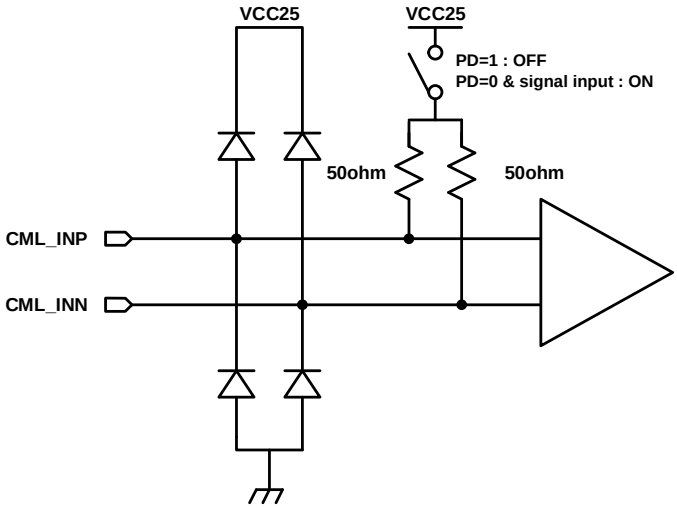


Figure 2. CML Input Schematic Diagram

Equivalent CML Output Diagram

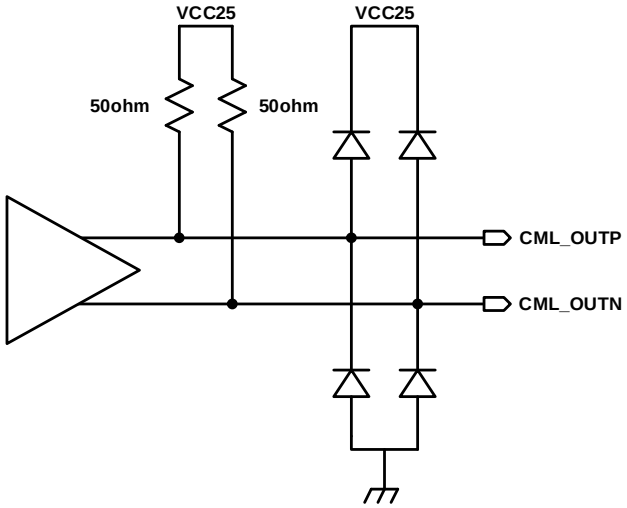


Figure 3. CML Output Schematic Diagram

Electrical Specification

LVCMOS DC Specification

Table 16. LVCMOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage	-	2.0	-	VCC33	V
VIL	Low Level Input Voltage	-	0	-	0.7	V
VOH	High Level Output Voltage	I_{oh}=-2mA	2.4	-	VCC33	V
VOL	Low Level Output Voltage	I_{ol}=8mA	0	-	0.4	V
IOZH	Output Leak Current High in Hi-Z State	-	-15	-	15	uA
IOZL	Output Leak Current Low in Hi-Z State	-	-15	-	15	uA

Level Control LVCMOS DC Specification

Table 17. Level Control LVCMOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{TH\_RaRd\_USB}$	Voltage Threshold for Detecting an Active Cable Attach	CURRENT_MODE1=0 CURRENT_MODE0=0 (Default USB)	0.15	0.2	0.25	V
$V_{TH\_RdOpen\_USB}$	Voltage Threshold for Detecting a UFP Attach		1.45	1.6	1.7	V
$V_{TH\_RaRd\_MED}$	Voltage Threshold for Detecting an Active Cable Attach	CURRENT_MODE1=0 CURRENT_MODE0=1 (Type-C Current 1.5A)	0.35	0.4	0.45	V
$V_{TH\_RdOpen\_MED}$	Voltage Threshold for Detecting a UFP Attach		1.45	1.6	1.7	V
$V_{TH\_RaRd\_HIGH}$	Voltage Threshold for Detecting an Active Cable Attach	CURRENT_MODE1=1 CURRENT_MODE0=0 (Type-C Current 3.0A)	0.72	0.8	0.85	V
$V_{TH\_RdOpen\_HIGH}$	Voltage Threshold for Detecting a UFP Attach		2.35	2.6	2.8	V
$V_{TH\_RaRd\_DEV}$	Voltage Threshold for Detecting an Active Cable Attach	CURRENT_MODE1=1 CURRENT_MODE0=1 (Used on Device side)	0.15	0.2	0.25	V
$V_{TH\_RdOpen\_DEV}$	Voltage Threshold for Detecting a UFP Attach		2.35	2.6	2.8	V
I_{IH_LC}	High Level Input Leak Current	VIN=5.5V	-100	-	100	uA
		VIN<2.5V	-15	-	15	uA
I_{IL_LC}	Low Level Input Leak Current	VIN=GND	-15	-	15	uA

3-Level LVCMOS DC Specification

Table 18. 3-Level LVCMOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{THL}	Low-Level Threshold Voltage	*	0.42	0.83	1.25	V
V_{THH}	High-Level Threshold Voltage	*	1.25	1.67	2.08	V
I_{IH_3L}	High Level Input Leak Current	VIN=VCC33	-100	-	100	uA
I_{IL_3L}	Low Level Input Leak Current	VIN=GND	-100	-	100	uA

*Must be tied for setting each level

Low: Tie 1kΩ ±5% to GND

Float: Leave pin open

High: Tie 1kΩ ±5% to VCC33

Open-Drain LVCMOS DC Specification

Table 19. Open-Drain LVCMOS DC/AC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low-level Input Voltage[1]	-	0	-	0.7	V
V_{IH}	High-level Input Voltage[1]	-	1.86	-	5.5	V
V_{OL1}	Low-level Output Voltage	3 mA sink current	-	-	0.4	V
I_{OL}	Low-level Output Current	V_{OL}=0.4V	20	-	-	mA
I_{IH}	High Level Input Leak Current	VIN=5.5V	-10	-	10	uA
I_{IL}	Low Level Input Leak Current	VIN=GND	-10	-	10	uA
C_I	Capacitance for Each I/O Pin	-	-	-	10	pF

Supply Current

Table 20. Supply Current

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCW	Active Mode Supply Current	PD=0,EQx*1=High DEEMx*1=High, OUTAMPx*1=High	-	-	170	mA
		PD=0,EQx*1=Float DEEMx*1=Low, OUTAMPx*1=Float	-	120	-	mA
ICCI	Unplug Mode Supply Current	PD=0, no output load is detected	-	3.0	4.0	mA
ICCS	Power Down Supply Current	PD=1	-	1.0	2.0	mA

*1 x=A, B

Receiver DC/AC Specification

Table 21. Receiver DC/AC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IN-DIFF-PP}$	AC Coupled Differential Input Peak to Peak Signal	10Gbps PRBS9	-	-	1200	mV
R_{RX-DC}	Receiver DC Common Mode Impedance	-	-	30	-	Ω
$R_{RX-DIFF-DC}$	DC Differential Impedance	-	72	100	120	Ω
$R_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0	-	25	-	-	kΩ
$RL_{RX-DIFF}$	Rx Differential Return Loss	0.05 to 5 GHz	-	-10	-	dB
RL_{RX-CM}	Rx Common Mode Return Loss	0.05 to 5 GHz	-	-6	-	dB
$V_{RX-EQ-LOW}$	Input Equalization, 2.0dB	EQx*1=Low	-	2	-	dB
$V_{RX-EQ-FLOAT}$	Input Equalization, 4.0dB	EQx*1=Float	-	4	-	dB
$V_{RX-EQ-HIGH}$	Input Equalization, 8.0dB	EQx*1=High	-	8	-	dB

*1 x=A, B

Transmitter DC / AC specifications

Table 22. Transmitter DC / AC specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Differential p-p Tx Voltage Swing	OUTAMPx*1=Float	0.8	1	1.2	V
$V_{TX-DIFF-PP-HIGH}$	High-Power Differential p-p Tx Voltage Swing	OUTAMPx*1=High	-	1.3	-	
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential p-p Tx Voltage Swing	OUTAMPx*1=Low	-	0.6	-	
$V_{TX-DE-RATIO-LOW}$	Tx De-emphasis Ratio	DEEMx*1=Low	-	-3.5	-	dB
$V_{TX-DE-RATIO-FLOAT}$	Tx De-emphasis Ratio	DEEMx*1=Float	-	-6	-	dB
$V_{TX-DE-RATIO-HIGH}$	Tx De-emphasis Ratio	DEEMx*1=High	-	-8.5	-	dB
T_{DE}	De-emphasis Width	-	-	100	-	ps
$T_{TX-DJ-DD}$	Deterministic Jitter	Loss=18dB@5GHz	-	0.25	-	UIpp
$T_{TX-RJ-DD}$	Random Jitter	-	-	0.5	-	ps RMS
$T_{TX-RISE-FALL}$	Tx Rise/Fall Time	20% to 80 %	-	40	-	ps
$T_{RF-MISMATCH}$	Tx Rise/Fall Mismatch	-	-	0.01	-	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss*2	0.05 to 5 GHz	-	-10	-	dB
RL_{TX-CM}	Tx Common Mode Return Loss*1	0.05 to 5 GHz	-	-6	-	dB
$R_{TX-DIFF-DC}$	DC Differential Impedance	-	80	100	120	Ω
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed during Receiver Detection	-	-	-	0.6	V
$V_{TX-DC-CM}$	Transmitter DC Common-mode Voltage	-	-	1.9	-	V
$V_{TX-CM-AC-PP\_ACTIVE}$	Transmitter AC Common-mode Voltage Active	-	-	-	100	mVpp
$I_{TX-SHORT}$	Transmitter Short-circuit Current Limit	-	-	20	60	mA
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	-	0	-	10	mV
$C_{TX-PARASITIC}$	Tx input capacitance	-	-	-	1.1	pF
$T_{PROPAGATION}$	Differential Propagation Delay	-	-	150	-	ps
$T_{MUX-SWITCH}$	Mux/Switch Time	-	-	10	-	us

*1 x=A, B
*2 Confirmed evaluation board

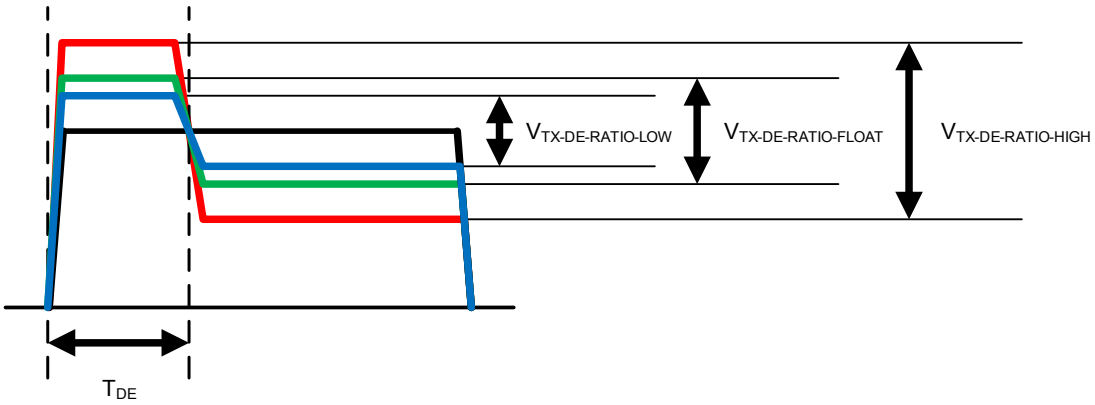
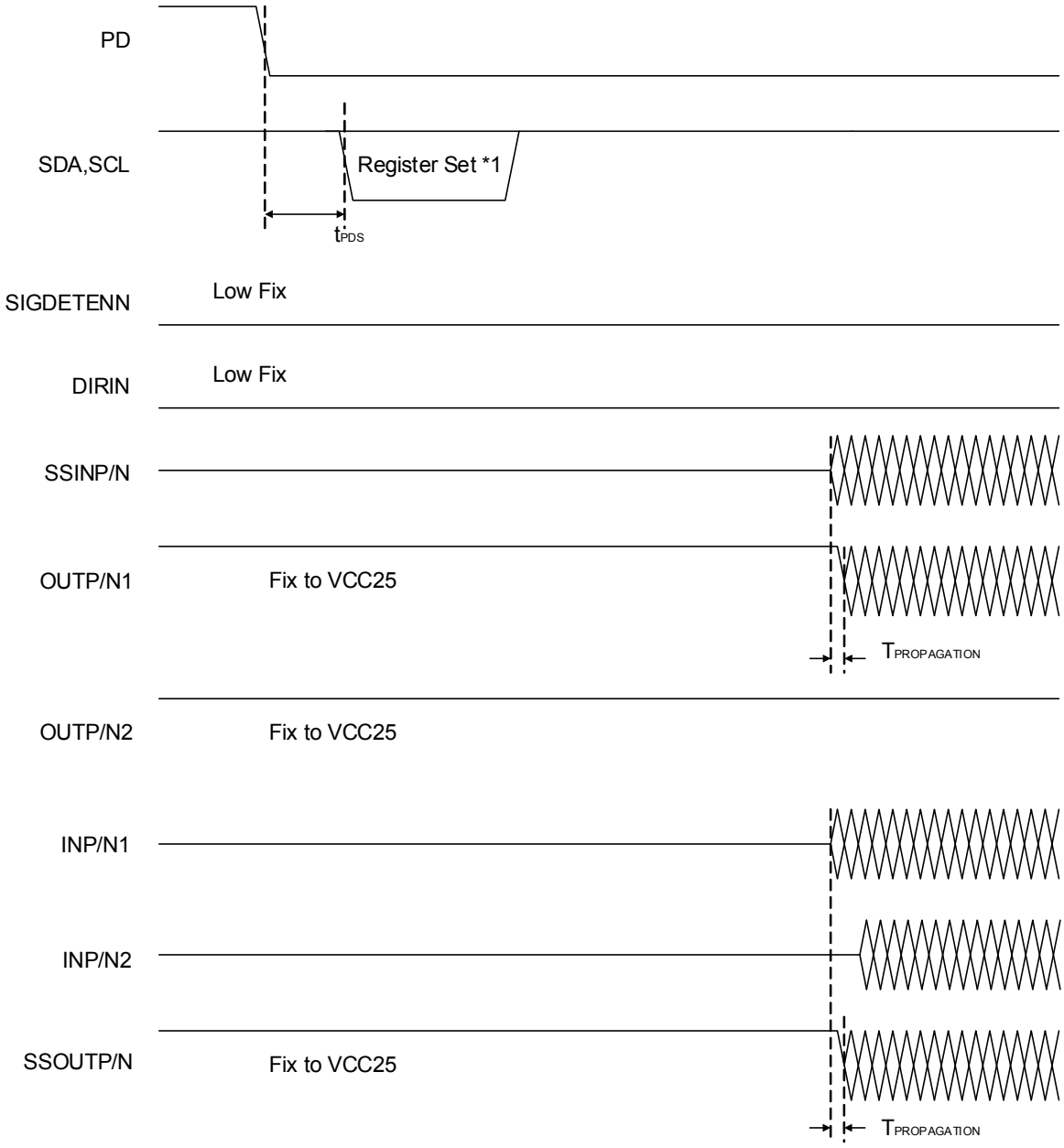
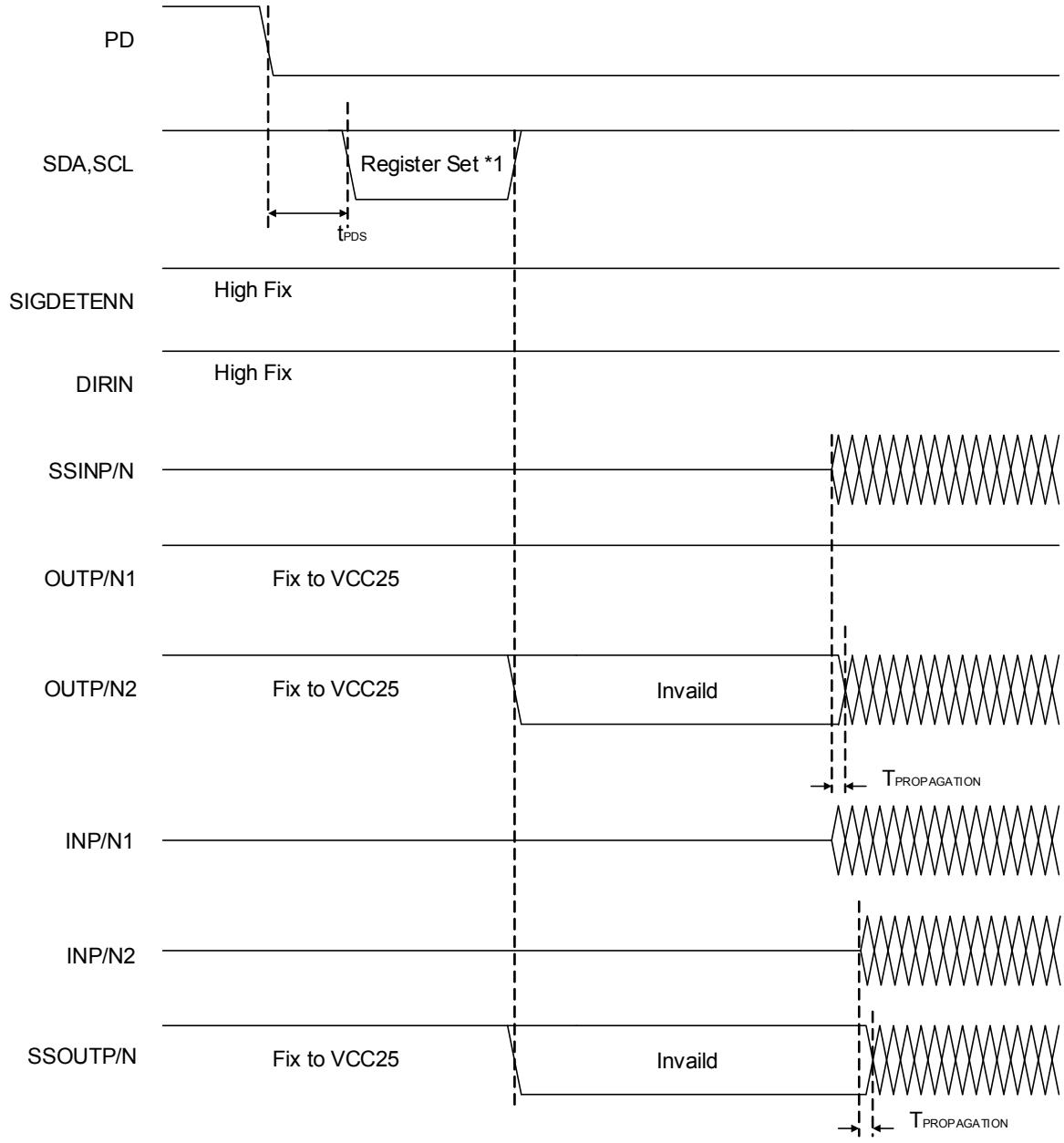


Figure 4. De-emphasis Level



*1 Refer to Table 7 and Table 9

Figure 5 Power on Sequence (Signal Detect Enable/Rx Detect Disable/CC logic Disable/Port 1 Active)



*1 Refer to Table 7 and Table 9

Figure 6 Power on Sequence (Signal Detect Disable/Rx Detect Disable/CC logic Disable/Port 2 Active)

2-wire serial I/F Electrical Characteristics

Table 23. Characteristics of the SDA and SCL bus line for 2-wire serial I/F

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCL}	SCL Clock Frequency	-	0	-	1	MHz
$t_{HD;STA}$	Hold Time (repeated) START Condition	After this period, the first clock pulse is generated.	0.26	-	-	us
t_{LOW}	Low Period of the SCL Clock	-	0.5	-	-	us
t_{HIGH}	High Period of the SCL Clock	-	0.26	-	-	us
$t_{SU;STA}$	Set-up Time for a Repeated START Condition	-	0.26	-	-	us
$t_{HD;DAT}$	Data Hold Time	-	0	-	-	us
$t_{SU;DAT}$	Data Set-up Time	-	50	-	-	ns
t_r	Rise Time of both SDA and SCL Signals	-	-	-	300	ns
t_f	Fall Time of both SDA and SCL Signals	-	-	-	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	-	0.26	-	-	us
t_{BUF}	Bus Free Time between a STOP and START Condition	-	0.5	-	-	us
t_{SP}	Pulse Width of Spikes Which Must be Suppressed by the Input Filter	-	-	-	50	ns
t_{PDS}	Required wait time from PD low to START condition	-	1	-	-	ms

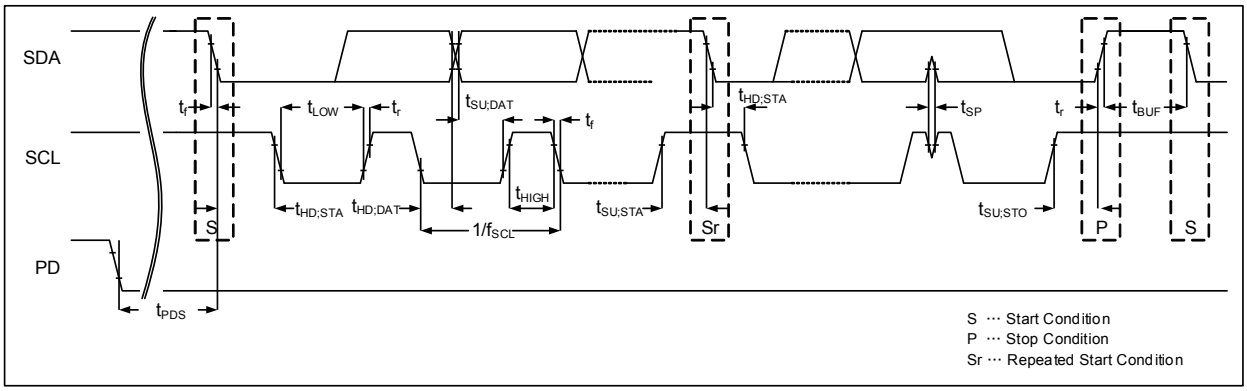
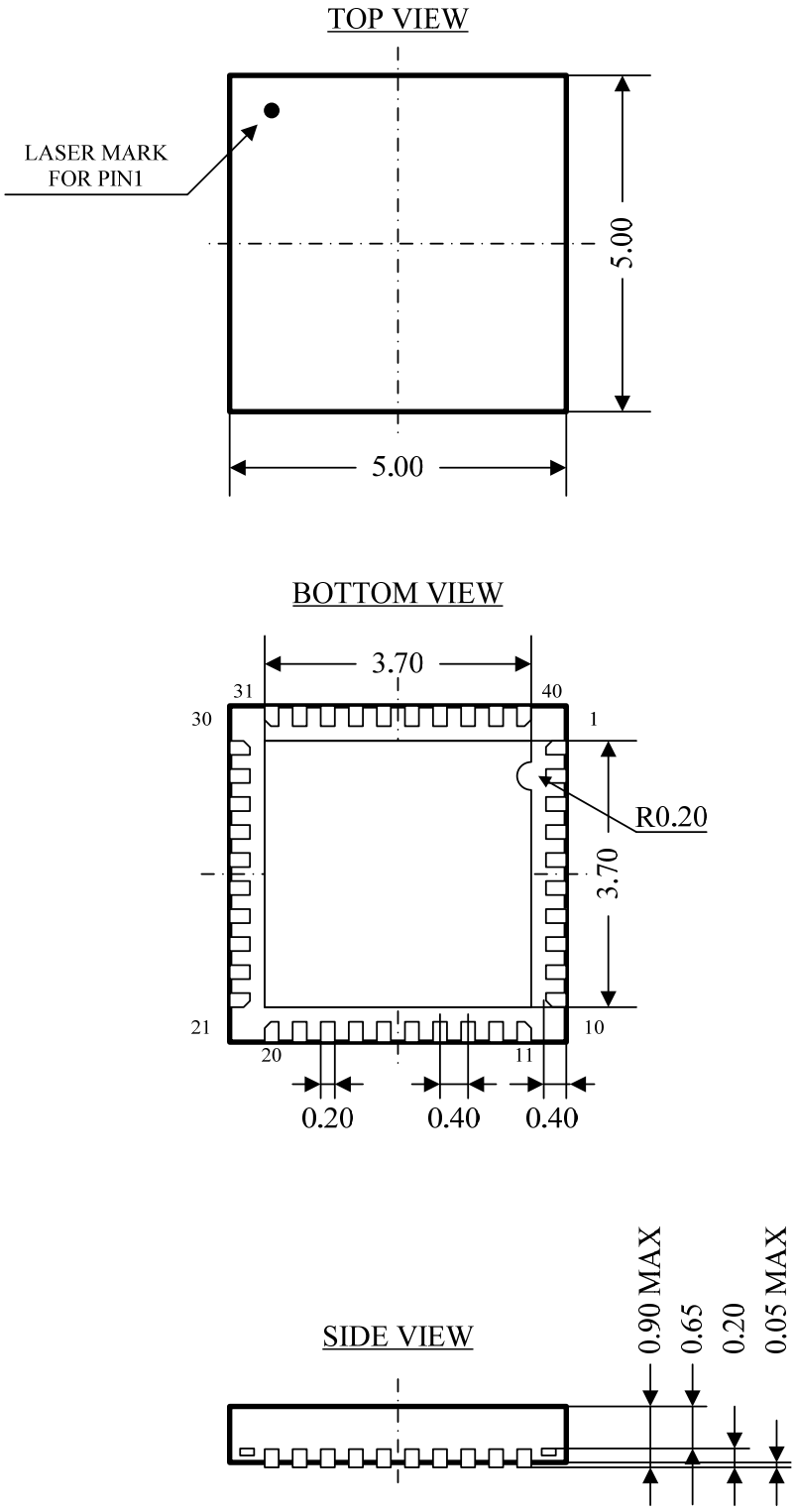


Figure 7. 2-Wire Serial Interface Timing Diagram

Package



Unit : mm

Figure 8. 40-pin QFN package physical dimension

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