THC63LVD823C

SMALL PACKAGE / 174MHz 27Bits LVDS Transmitter

General Description

The THC63LVD823C transmitter is designed to support pixel data transmission between Host and Flat Panel Display and Dual Link transmission between Host and Flat Panel Display up to 1080p/WUXGA, 1920x1440(RB) resolutions.

The THC63LVD823C converts 27bits (RGB 8 bits + Hsync, Vsync, DE) of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin.

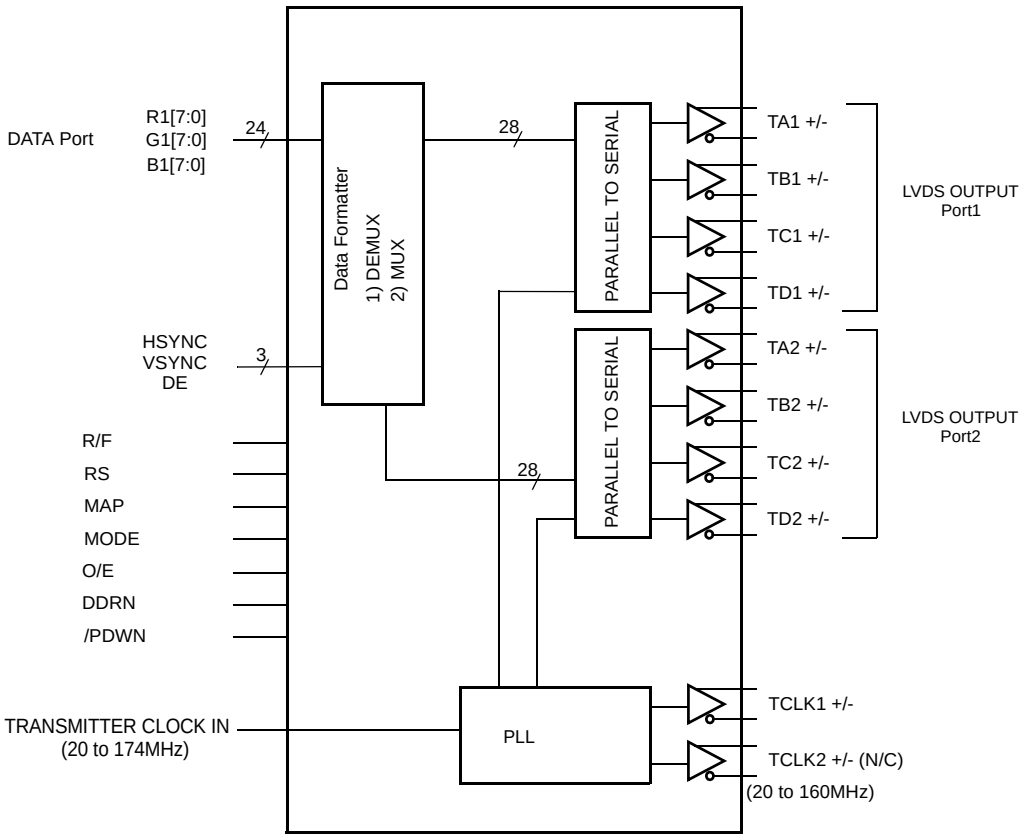
For dual LVDS out, LVDS clock frequency of 87MHz, 51bits of RGB data are transmitted at an effective rate of 609Mbps per LVDS channel.

For single LVDS out, LVDS clock frequency of 174MHz, 27bits of RGB data are transmitted at an effective rate of 1218Mbps per LVDS channel.

Features

- 3.3V single power supply
- 7mm x 7mm/72pin/0.65mm pitch/TFBGA package
- Wide dot clock range suited for
  TV Signal: up to 1080p (74.25MHz dual)
  PC Signal: up to 1920x1440 (86MHz dual)
- 1.2V / 1.8V/ 2.5V / 3.3V CMOS inputs are supported with VREF input from RS pin
- LVDS swing reducible by RS-pin to reduce both EMI and power consumption
- PLL requires No external components
- Flexible Input/Output mode
  1. Single TTL IN, Single/Dual LVDS OUT
  2. Double edge Single TTL IN/Dual LVDS OUT
- 2 LVDS data mapping for simplifying PCB layout
- Power down mode
- Input clock triggering edge selectable by R/F pin

Block Diagram



Pin Out (top view)

TOP VIEW

	1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1+	TD1+	TA2+	TB2+	TC2+	TCLK2+	A
B	TA1-	TB1-	TC1-	TCLK1-	TD1-	TA2-	TB2-	TC2-	TCLK2-	B
C	Reserved3	N/C	Reserved1	GND	LVDS VCC	GND	PLL VCC	TD2-	TD2+	C
D	R11	R10	LVDS VCC				GND	/PDWN	O/E	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				Reserved2	RS	CLKIN	F
G	R17	R16	VCC	GND	VCC	GND	VCC	R/F	DE	G
H	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	H
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
	1	2	3	4	5	6	7	8	9	

Pin Description

Pin Name	Pin #	Type	Description
TA1+, TA1-	A1,B1	LVDS OUT	The 1st Link. The 1st pixel output data when Dual-Link.
TB1+, TB1-	A2,B2		
TC1+, TC1-	A3,B3		
TD1+, TD1-	A5,B5		
TCLK1+, TCLK1-	A4,B4	LVDS OUT	LVDS Clock Out for 1st and 2nd Link.
TA2+, TA2-	A6,B6	LVDS OUT	The 2nd Link. These pins are disabled when Single Link.
TB2+, TB2-	A7,B7		
TC2+, TC2-	A8,B8		
TD2+, TD2-	C9,C8		
TCLK2+, TCLK2-	A9,B9	LVDS OUT	Additional LVDS Clock Out. Identical to TCLK1+,-. No connect if not used.
R17 ~ R10	G1,G2,F1,F2 E1,E2,D1,D2	IN	The 1st Pixel Data Inputs.
G17 ~ G10	J4,H4,J3,H3 J2,H2,J1,H1		
B17 ~ B10	J8,H8,J7,H7 J6,H6,J5,H5		
DE	G9	IN	Data Enable Input.
VSYNC	H9	IN	Vsync Input.
HSYNC	J9	IN	Hsync Input.
CLKIN	F9	IN	Clock Input.
R/F	G8	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
RS	F8	IN	LVDS swing mode, V_{REF} select. See Fig4 - 5. RS: V_{IHM} — LVDS Swing: 350mV — Small Swing Input Support: N/A RS: V_{IMM} — LVDS Swing: 350mV — Small Swing Input Support: RS=V_{REF}[a] RS: V_{ILM} — LVDS Swing: 200mV — Small Swing Input Support: N/A a. V_{REF} is Input Reference Voltage.
MAP	E8	IN	LVDS mapping table select. See Fig7 to 8 and Table4 to 7. MAP: V_{IHM} — Mapping Mode: Mapping MODE1 MAP: V_{ILM} — Mapping Mode: Mapping MODE2 MAP: V_{IMM} — Mapping Mode: Reserved
MODE	E7	IN	Pixel Data Mode. MODE: L — Modes: Dual Link (Single-in/Dual-out) MODE: H — Modes: Single Link (Single-in/Single-out)
O/E	D9	IN	Output enable. H: Output enable, L: Output disable (all outputs are Hi-Z).

Pin Description (Continued)

Pin Name	Pin #	Type	Description
/PDWN	D8	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
Reserved1	C3	IN	Must be tied to GND.
Reserved2	F7	IN	Must be tied to GND.
Reserved3	C1	IN	Must be tied to GND.
DDRN	E9	IN	DDR function is active when MODE = L (Single-in/Dual-out mode). Open or H: DDR (Double Edge input) function disable. L: DDR (Double Edge input) function enable.
N/C	C2		Must be Open.
VCC	G3,G5,G7	Power	Power Supply Pins for TTL inputs and digital circuitry.
LVDSVCC	C5,D3	Power	Power Supply Pins for LVDS Outputs.
PLLVCC	C7	Power	Power Supply Pin for PLL circuitry.
GND	C4,C6,D7,E3, F3,G4,G6,	Ground	Ground Pins for TTL inputs and digital circuitry.

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Transmitter Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	1.6W

Recommended Operating Conditions

Parameter				Min.	Typ	Max	Units
All Supply Voltage				3.0	3.3	3.6	V
Operating Ambient Temperature				-20		70	°C
Clock Frequency	MODE=L Single-in/Dual-out	Single Edge Input (DDRN =Open/H)	Input	40		174	MHz
			LVDS Output	20		87	MHz
		Double Edge Input (DDRN=L)	Input	20		80	MHz
			LVDS Output	20		80	MHz
	MODE=H Single-in/Single-out		Input	20		160	MHz
			LVDS Output	20		160	MHz

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = VCC=PLLVCC=LVDSVCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}[a]	High Level Data Input Voltage	RS=V_{IHM}or V_{ILM}	2.0		V_{CC}	V
		RS=V_{IMM}	V_{REF}[b]+0.1			V
V_{IL}[a]	Low Level Data Input Voltage	RS=V_{IHM}or V_{ILM}	GND		0.8	V
		RS=V_{IMM}			V_{REF}-0.1	V
V_{IHC}[c]	High Level Control Input Voltage		2.0		V_{CC}	V
V_{ILC}[c]	Low Level Control Input Voltage		GND		0.8	V
V_{IHM}[d]	High Level Control Input Voltage		0.8V_{CC}		V_{CC}	V
V_{IMM}[d]	Middle Level Control Input Voltage		0.6		1.4	V
V_{ILM}[d]	Low Level Control Input Voltage		GND		0.08V_{CC}	V
I_{INC}	Input Current (except DDRN)	GND ≤ V_{IN} ≤ V_{CC}			±10	μA
I_{INCD}	Input Current (Only DDRN)	GND ≤ V_{IN} ≤ V_{CC}			±20	μA

a. CLKIN,R10~R17,G10~G17,B10~B17,DE,HSYNC,VSYNC
b. V_{REF} is input voltage of RS pin.
c. R/F,DDRN,MODE,O/E,/PDWN
d. RS,MAP

LVDS Transmitter DC Specifications

V_{CC} = VCC=PLLVCC=LVDSVCC

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS= V_{CC}	250	350	450	mV
			Reduced swing RS= GND	120	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=GND, RL=100Ω				-24	mA
I_{OZ}	Output TRI-State current	/PDWN=GND, VOUT=GND to V_{CC}				±10	μA

Electrical Characteristics (Continued)

Supply Current

V_{CC} = VCC=PLLVCC=LVDSVCC

Symbol	Parameter	Condition			Typ.	Max.	Units
I_{TCCW}	Transmitter Supply Current (Worst Case Pattern) Fig1.	RL=100Ω CL=5pF RS=V_{CC}	MODE=H Single-in/Single-out	CLKIN=65MHz		86	mA
				CLKIN=85MHz		100	mA
				CLKIN=135MHz		122	mA
			MODE=L Single-in/Dual-out DDRN=H or Open DDR Input Off	CLKIN=65MHz		114	mA
				CLKIN=85MHz		116	mA
				CLKIN=135MHz		155	mA
				CLKIN=150MHz		168	mA
			MODE=L Single-in/Dual-out DDRN=L DDR Input On	CLKIN=32.5MHz		114	mA
				CLKIN=42.5MHz		118	mA
				CLKIN=67.5MHz		155	mA
				CLKIN=75MHz		167	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = Fixed L or H				50	μA

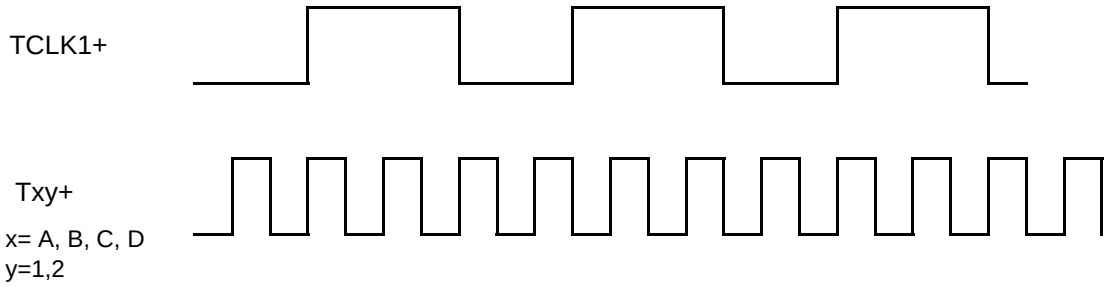


Fig1. Test Pattern
(LVDS Output Full Toggle Pattern)

Switching Characteristics

V_{CC} = VCC=PLLVCC=LVDSVCC

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{TCIP}	CLK IN Period(Fig4,5)		5.74		50	ns
t_{TCH}	CLK IN High Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLK IN Low Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN(Fig4,5)		2.5			ns
t_{TH}	TTL Data Hold from CKL IN(Fig4,5)		0.0			ns
t_{TCOP}	CLK OUT Period(Fig6)		6.25		50	ns
t_{LVT}	LVDS Transition Time(Fig2)			0.6	1.5	ns
t_{TOP1}	Output Data Position0 (Fig6)	t_{TCOP} = 7.4ns~20ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (Fig6)		$\frac{t_{TCOP}}{7} - 0.15$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP6}	Output Data Position2 (Fig6)		$2\frac{t_{TCOP}}{7} - 0.15$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP5}	Output Data Position3 (Fig6)		$3\frac{t_{TCOP}}{7} - 0.15$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP4}	Output Data Position4 (Fig6)		$4\frac{t_{TCOP}}{7} - 0.15$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP3}	Output Data Position5 (Fig6)		$5\frac{t_{TCOP}}{7} - 0.15$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP2}	Output Data Position6 (Fig6)		$6\frac{t_{TCOP}}{7} - 0.15$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TPLL}	Phase Lock Time(Fig3)				10.0	ms
t_{DEINT}	DE input period (Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE=L, DDRN =Open or H)		$4t_{TCIP}$	tTCIP*(2n) [a]		ns
t_{DEH}	DE High time (Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE=L, DDRN =Open or H)		$2t_{TCIP}$	tTCIP*(2m)[a]		ns
t_{DEL}	DE Low time(Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE=L, DDRN =Open or H)		$2t_{TCIP}$			ns

a. Refer to Fig3-1 for details.

AC Timing Diagrams

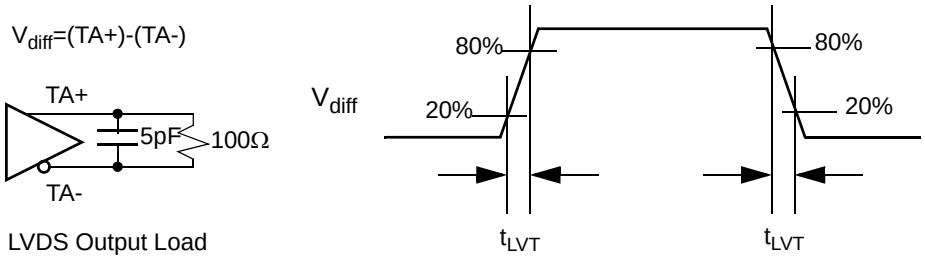


Fig2. LVDS Output Load and Transition Time

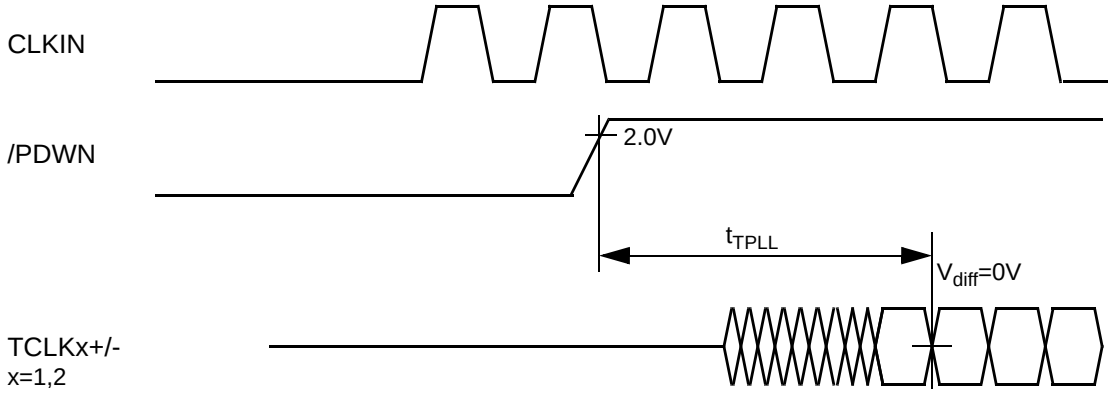
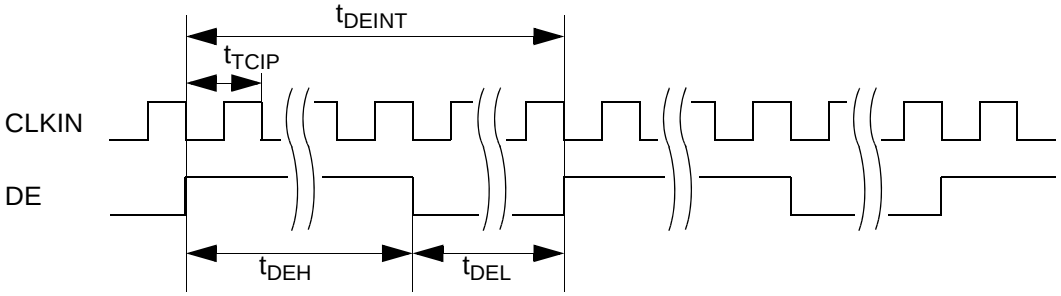


Fig3. PLL Lock Time



Note: In single-in/dual-out, DDR off mode (MODE=L, DDRN =Open or H), the period between rising edges of DE (t_{DEINT}), high time of DE (t_{DEH}) should always satisfy following equations.

t_{DEH} = tTCIP * (2m)

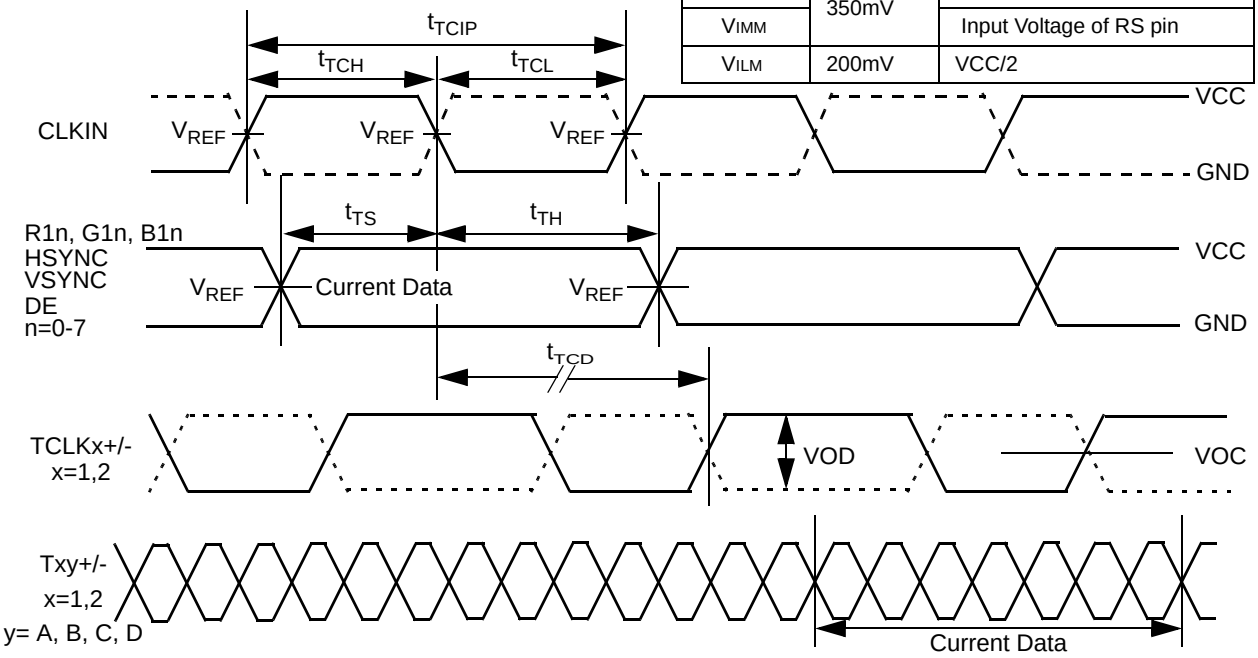
t_{DEINT} = tTCIP * (2n)

m, n =integer

Fig3-1. Single IN / Dual OUT, DDR off mode DE input timing

AC Timing Diagrams (Continued)

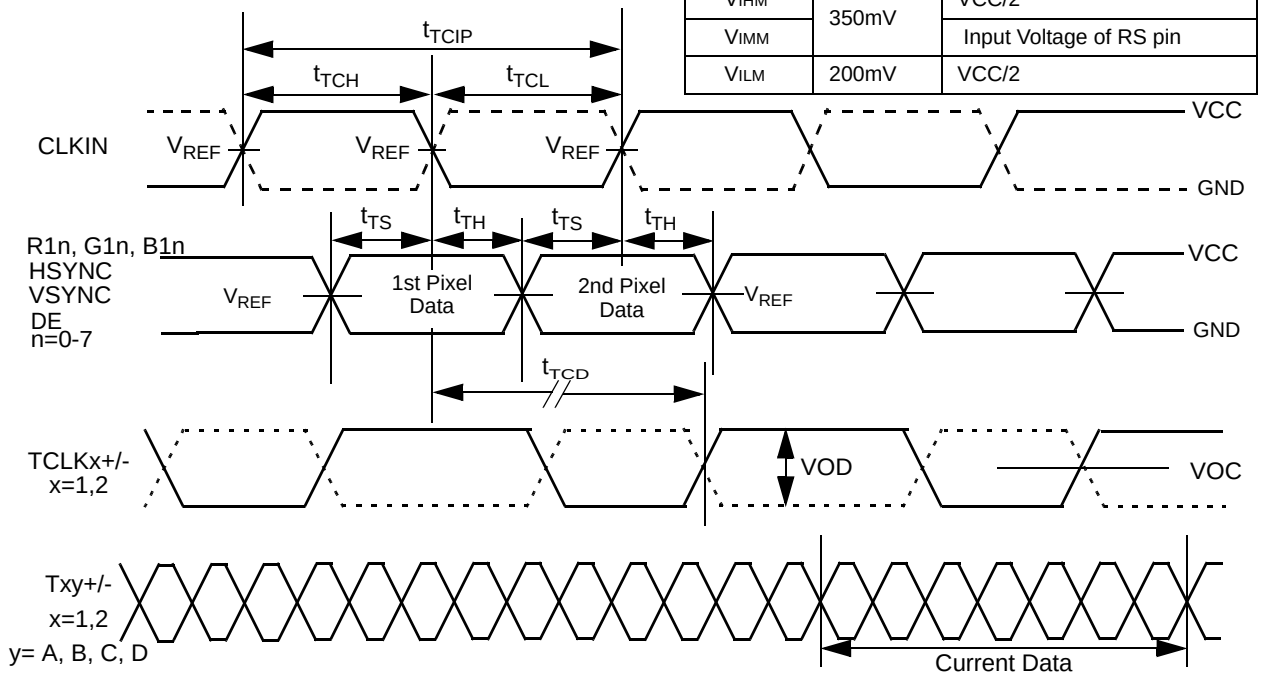
RS pin	VOD	VREF
VIHM	350mV	VCC/2
VIMM		Input Voltage of RS pin
VILM	200mV	VCC/2



Note:
CLKIN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line.

Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing

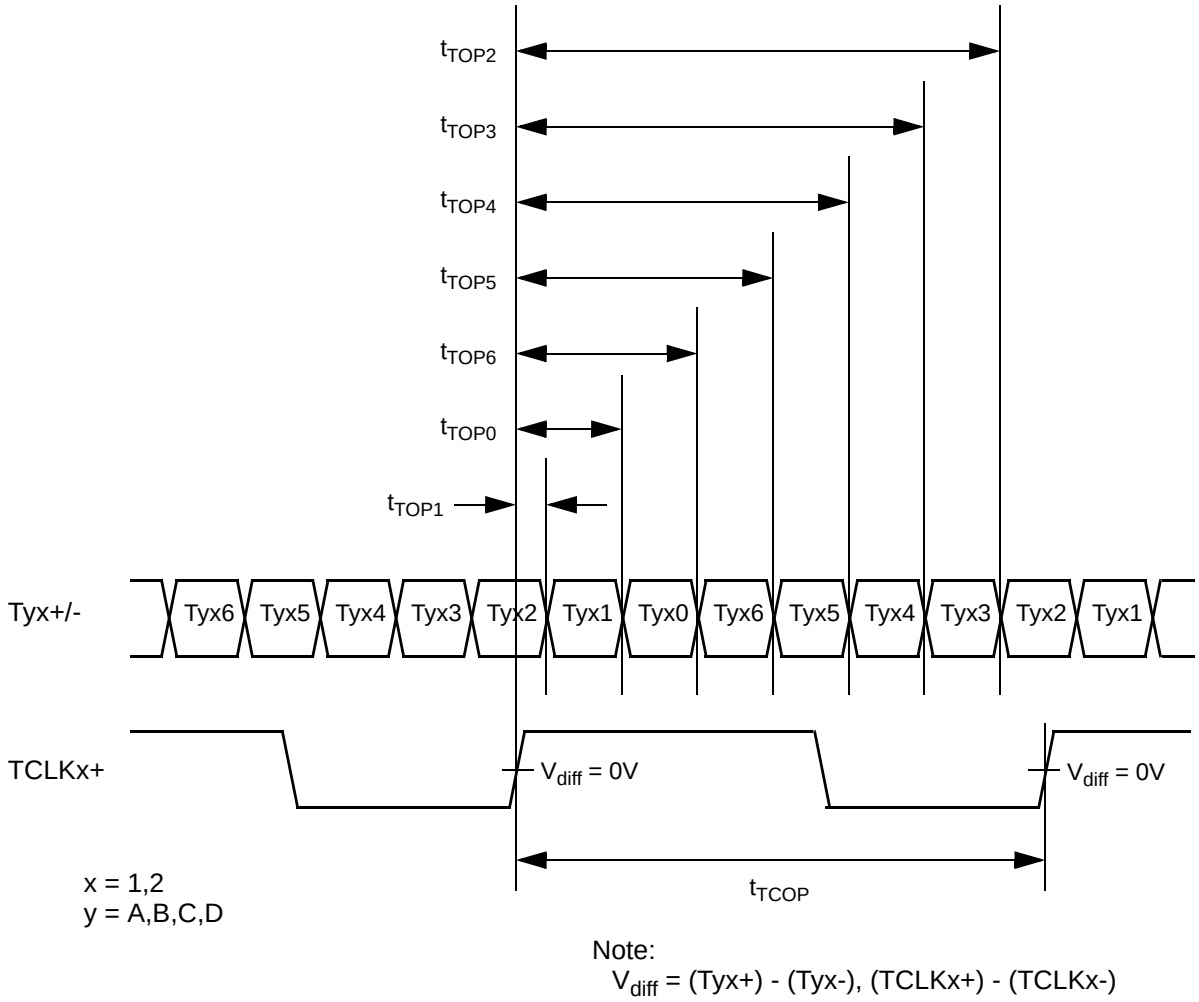
RS pin	VOD	VREF
VIHM	350mV	VCC/2
VIMM		Input Voltage of RS pin
VILM	200mV	VCC/2



Note:
CLKIN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line.

Fig5. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode (DDR) MODE=L,DDRN=L

AC Timing Diagrams (Continued)



Note:
V_{diff} = (Tyx+) - (Tyx-), (TCLKx+) - (TCLKx-)

Fig6. LVDS Output Data Position

Input Data Mapping

•Table1. TTL/CMOS Input Data Mapping

Data Signals	Transmitter Input Pin Names
R0	R10
R1	R11
R2	R12
R3	R13
R4	R14
R5	R15
R6	R16
R7	R17
G0	G10
G1	G11
G2	G12
G3	G13
G4	G14
G5	G15
G6	G16
G7	G17
B0	B10
B1	B11
B2	B12
B3	B13
B4	B14
B5	B15
B6	B16
B7	B17

LVDS Output Data Mapping

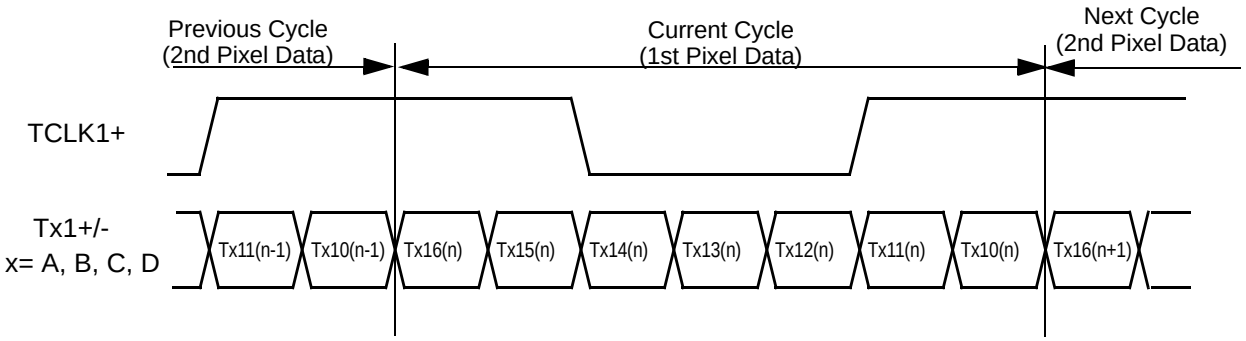


Fig7. TTL Data Inputs Mapped to LVDS outputs
MODE= H (Single-out Mode)

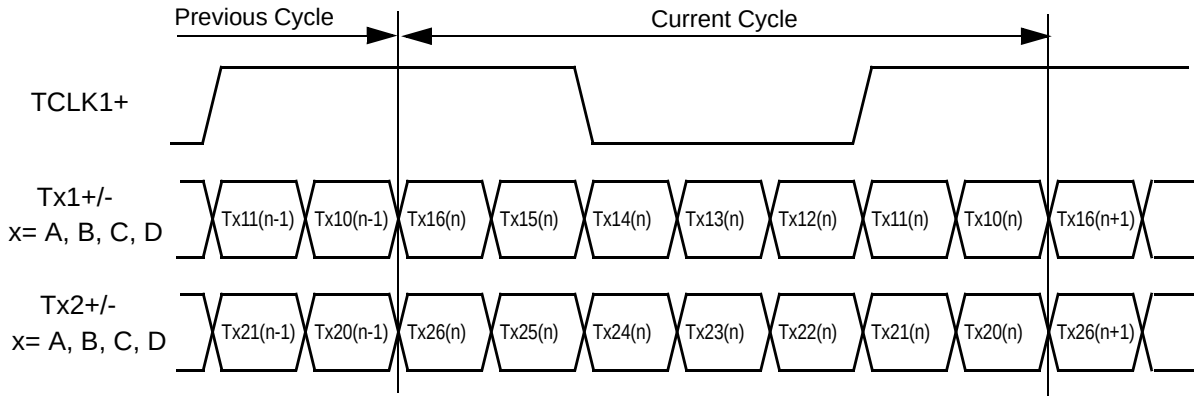


Fig8. TTL Data Inputs Mapped to LVDS outputs
MODE= L (Dual-out Mode)

LVDS Output Data Mapping (Continued)

•Table2. LVDS Output Data Mapping (Single-in/Single-out, MODE=H)

LVDS Output Data	Mapping Mode (Input Pin Name)	
	Mode1 MAP=H	Mode2 MAP=L
TA10	R12	R10
TA11	R13	R11
TA12	R14	R12
TA13	R15	R13
TA14	R16	R14
TA15	R17	R15
TA16	G12	G10
TB10	G13	G11
TB11	G14	G12
TB12	G15	G13
TB13	G16	G14
TB14	G17	G15
TB15	B12	B10
TB16	B13	B11
TC10	B14	B12
TC11	B15	B13
TC12	B16	B14
TC13	B17	B15
TC14	HSYNC	HSYNC
TC15	VSYNC	VSYNC
TC16	DE	DE
TD10	R10	R16
TD11	R11	R17
TD12	G10	G16
TD13	G11	G17
TD14	B10	B16
TD15	B11	B17
TD16	N/A	N/A

LVDS Output Data Mapping (Continued)

•Table3. LVDS Output Data Mapping (Single-in/Dual-out, DDR On/Off, MODE=L, DDRN =Open/H/L)

LVDS Output Data (1st Link)	Mapping Mode (Input Pin Name)		LVDS Output Data (2nd Link)	Mapping Mode (Input Pin Name)	
	Mode1 MAP=H	Mode2 MAP=L		Mode1 MAP=H	Mode2 MAP=L
TA10	R12	R10	TA20	R12	R10
TA11	R13	R11	TA21	R13	R11
TA12	R14	R12	TA22	R14	R12
TA13	R15	R13	TA23	R15	R13
TA14	R16	R14	TA24	R16	R14
TA15	R17	R15	TA25	R17	R15
TA16	G12	G10	TA26	G12	G10
TB10	G13	G11	TB20	G13	G11
TB11	G14	G12	TB21	G14	G12
TB12	G15	G13	TB22	G15	G13
TB13	G16	G14	TB23	G16	G14
TB14	G17	G15	TB24	G17	G15
TB15	B12	B10	TB25	B12	B10
TB16	B13	B11	TB26	B13	B11
TC10	B14	B12	TC20	B14	B12
TC11	B15	B13	TC21	B15	B13
TC12	B16	B14	TC22	B16	B14
TC13	B17	B15	TC23	B17	B15
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R10	R16	TD20	R10	R16
TD11	R11	R17	TD21	R11	R17
TD12	G10	G16	TD22	G10	G16
TD13	G11	G17	TD23	G11	G17
TD14	B10	B16	TD24	B10	B16
TD15	B11	B17	TD25	B11	B17
TD16	N/A	N/A	TD26	N/A	N/A

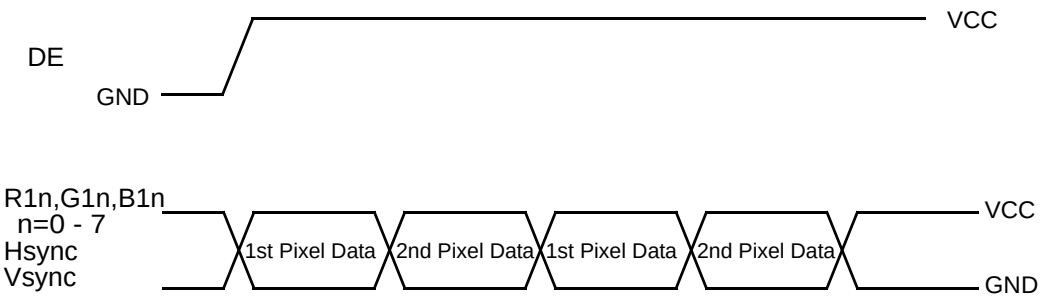


Fig9. The decision rule of 1st Pixel data in Single IN/Dual Out DDR Off
(MODE=L, DDRN =Open or H)

Note

1)Cable Connection and Disconnection

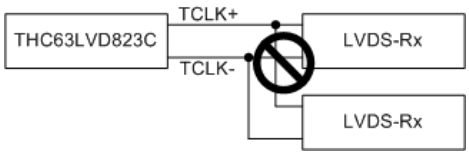
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVD823C and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

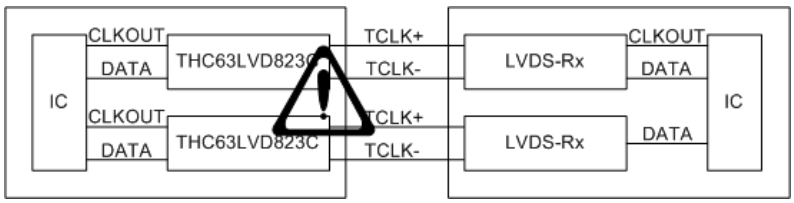
3)Multi Drop Connection

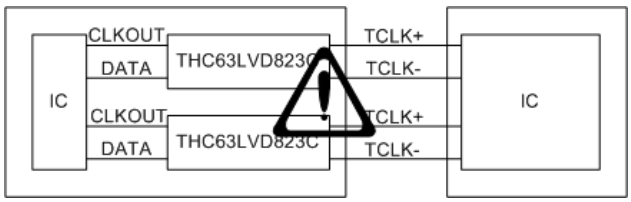
Multi drop connection is not recommended.



4)Asynchronous use

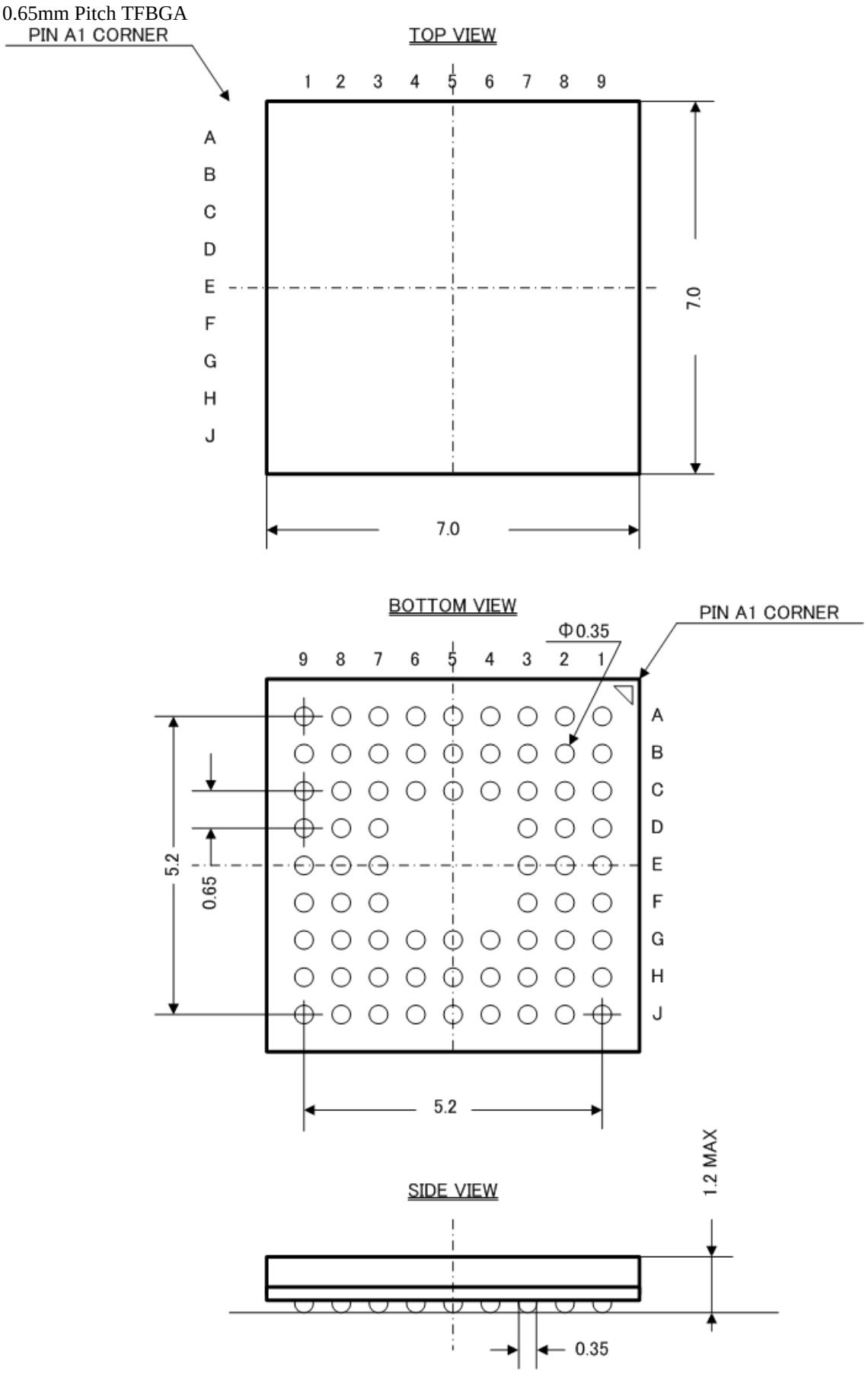
Asynchronous use such as following systems are not recommended.





Package

0.65mm Pitch TFBGA



Notices and Requests

1.)The product specifications described in this material are subject to change without prior notice.
2.)The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3.)This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4.)Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5.)This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6.)Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7.)Please note that this product is not designed to be radiation-proof.
8.)Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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