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Chip Set Enables Embedded GPS

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**Computer-Aided
Engineering
Issue**

cover story

Chip Set Adds Embedded GPS

Two companies team to provide a “universal solution” for embedded Global Positioning System (GPS) capabilities in portable wireless products.



Global-positioning technology is finding its way into more and more wireless products, sometimes by Federal mandate. The E911 ruling by the United States Federal Communications Commission (FCC), which requires position-location capability in new cellular telephones, has brought GPS technology to millions of consumers. As those users become more

familiar with the capabilities of GPS, the demand for positioned-based data is certain to accelerate. 2.5G and 3G wireless networks promise to provide the increased data capacity these new location-based services will demand. In response to increased demands for embedded GPS functionality, two California companies have joined forces to create a low-cost, low-power Global Positioning System (GPS) chip set to address the challenge.

The chip set teams the UPB1008K GPS receiver integrated circuit (IC) from California Eastern Laboratories (Santa Clara, CA) with the Opus One system-on-a-chip (SoC) baseband IC from eRide (San Jose, CA). The two-chip set forms a “universal hardware” solution in that it operates independently of wireless interface standards and independently of the host product’s central processing unit (CPU) and operating system. The advanced GPS chip set delivers fast acquisition times, high sensitivity even when used indoors, and software designed to make the integration into wireless products easier than ever before. The design promises faster time-to-market, lower manufacturing costs, and ultimately, lower cost to consumers.

The UPB1008K (Fig. 1) combines a low-noise amplifier (LNA), a double-conversion downconverter, and a phase-lock-loop (PLL) frequency synthesizer. It also includes 2-b analog-to-digital converters (ADCs) to generate 2-b digitized outputs and can operate on supply voltages as low as +2.7 VDC (the nominal supply voltage is +3 VDC). In the downconversion process, the first intermediate frequency (IF) is at 175.164 MHz while the second IF is at 132 kHz.

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An on-chip IF automatic-gain-control (AGC) amplifier provides an adjustable gain range of more than 30 dB. Fabricated with a 25-GHz cutoff-frequency silicon bipolar process, the IC is supplied in a 36-pin QFN package.

The baseband IC (Fig. 2) features operation at +1.8-VDC core and +3.3-VDC I/O, with peak power of only 300 mW for the first indoor fix (performing high sensitivity searching of all satellite with up to 44,000 code and frequency hypotheses), and then reduced power of 100 to 200 mW power for subsequent fixes (continuing to track all satellites with fewer hypotheses for weak signals or conventionally for stronger signals to acquire the 50-b/s GPS data message), and 30 mW in standby mode. The IC supports -155 dBm indoor sensitivity, and requires only 3 to 5 s to gain a satellite fix outdoors and only 10 to 20 s indoors to capture the needed satellite signals for a GPS location fix. The IC is supplied in a 9×9 -mm ball-grid-array (BGA) package.

The Opus One baseband IC combines state machines, peripheral devices, and a low-frequency clock for high-performance operation without need for external memory.

The IC features two state machines. The first, the Opus State Machine (OSM), handles all codes and internal frequency generation and correlation and provides the interface between baseband hardware and software. The second, the Firmware State Machine (FSM), incorporates an indoor state machine (IDSM), an outdoor state machine (ODSM), and a time-tracking state machine. The ISM supports indoor sensitivity to -155 dBm in 1-s dwells. The ODSM is designed to search all 32 GPS satellites with -142 -dBm sensitivity using a search window of two 10-ms dwells. The TSM collects the navigational data and provides synchronous measurements so that GPS time and navigation data can be decoded and assimilated (allowing the Opus One to be used all as a reference station for the eRide reference network).

The baseband IC has an effective 44,000 correlates in each 10-ms search



1. The UPB1008K GPS IC packs an LNA, frequency downconverter, and PLL frequency synthesizer into a 36-pin QFN enclosure.



2. The Opus One baseband IC combines state machines, peripheral devices, and a low-frequency clock in a 10×10 -mm ball-grid-array (BGA) package.

window, with correlation performed in the time domain rather than the frequency domain. By doing these correlations and configurations in the time domain rather than frequency domain, Opus allows more efficient use of hardware and memory across the different tracking modes. As a result, the baseband processor can perform correlation of as many as 120 satellites in parallel. This search power can be configured to perform the equivalent correlation of up to 130 frequency hypotheses in parallel. The use of two different state machines in the Opus One IC addresses the challenge of cross correlation, which is the mixing of fading or low-level signals with higher-level signals as well as the mixing of multipath signals.

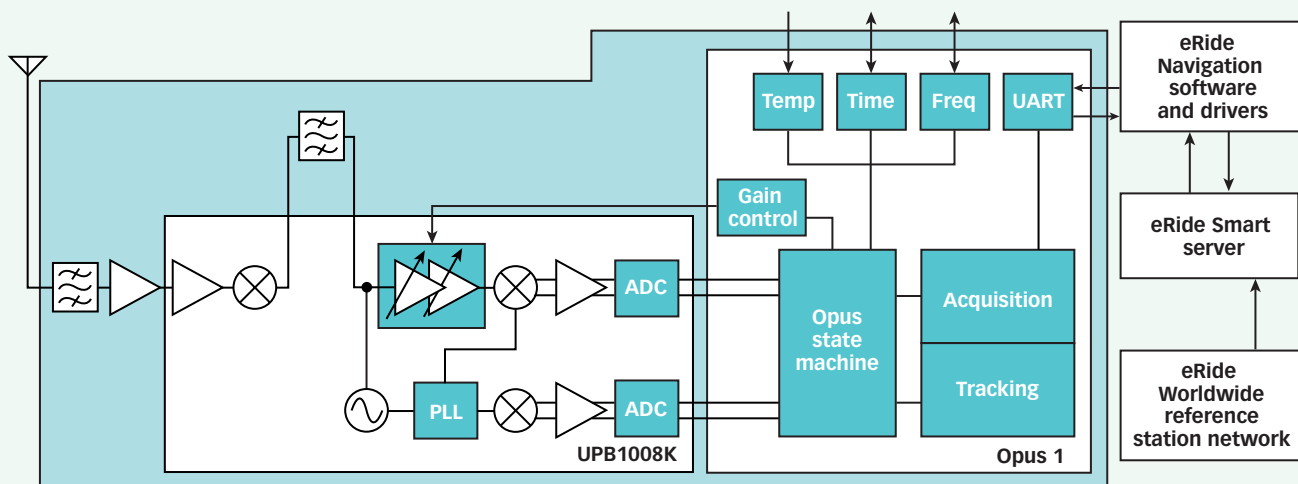
Other Opus One firmware logic handles all of the peripheral support oper-

ations. It provides a real time clock, synchronizes time and frequency across platforms, compensates for temperature, and using patented software, and compensates for crystal-oscillator drift without the need for input from outside the receiver (allowing for the use of lower-cost crystal oscillators with the chip set).

The time required to integrate a weak GPS signal is often too long to be commercially practical. To speed processing, the Opus chip automatically optimizes its search and tracking power based on the starting information available. On a cold start (no starting information), Opus One searches for all 32 GPS satellites, each of which has its own unique pseudo-random noise (PRN) code. The baseband processor begins with quick wide-bandwidth searches, then automatically transitions to time-track to collect navigation data. If more starting information is available, its search power is automatically configured to look for satellites in a narrower bandwidth, effectively increasing its power to deliver higher sensitivity. This results in practical times for the first fix: 3 to 5 s outdoors and 10 to 20 s indoors. Opus One also has the ability to track the carrier phase and demodulate the 50-b/s GPS Navigation message. This allows Opus One to fix autonomously from aiding data.

To further speed navigational computations, the eRide software uses its own portable math libraries. Its floating-point library has the ability to do sub-meter positioning without an external floating point or transcendental functions. It also has the ability to do fixed-point calculations, which speeds up matrix operations, allowing parallel fix solutions for integrity monitoring.

The unique software is designed to require very little computational power on the part of the host CPU, and very little random-access memory (RAM). Besides being efficient, it facilitates the integration of GPS capability into mobile platforms with limited available processing capability. It requires just one task slot and one serial interrupt from



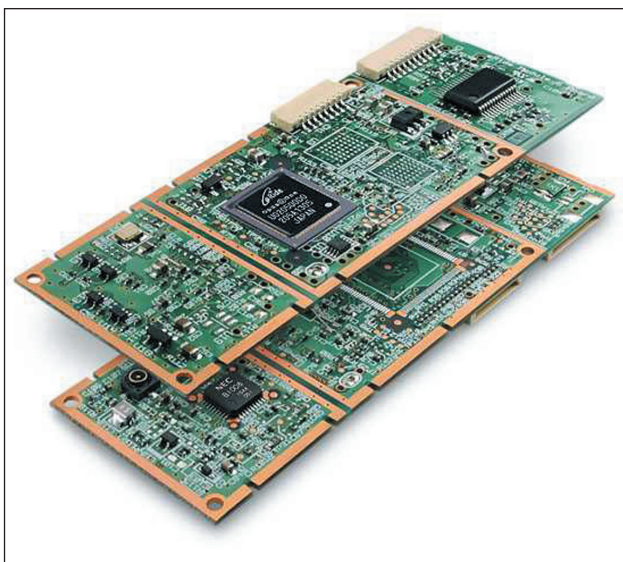
3. A complete embedded GPS solution consists of the UPB1008K and Opus One ICs, a few external components, and software and network support.

the host platform schedule in order to operate.

The software's Omni mode is a near-autonomous GPS solution with operation in either assisted or autonomous modes. In assisted mode, satellite positioning and timing data, along with an approximate position of the receiver, are all provided by the network via eRide's Smart Server and Worldwide Reference Network. In autonomous mode, aiding data are not needed. This network gathers, processes, and stores navigational data and satellite orbital models, and then communicates the data to a customer via TCP/IP, SMS, or control channels. The Omni software is designed to operate autonomously, but then tap into aiding data when needed. The instantaneous availability of this stored reference data—with no real-time interruption—helps reduce the time to first fix and ensure high accuracy.

From simple positioning systems to major enterprise-level data delivery networks, this flexible architecture (Fig. 3) makes it possible to scale the software to match the bandwidth of the host application. Integration is simple and straightforward: The chip set connects to the host processor via a two-way RS-232 interface. Navigation software and drivers are written in C language making them easy to port to the host CPU software. The Smart Server and Worldwide Reference

4. Complete evaluation boards are available to test the performance of the two GPS ICs.



Network use the open Java Messaging Service (JMS) enabling deployment into virtually any wireless infrastructure, independent of its air-interface standard.

Typically, the GPS chip set requires just 6 million instructions per second (MIPS) processing power available from the host CPU, with 32 kB of available RAM, and 100 kb of instruction memory to perform position, velocity and timing calculations using eRide's proprietary protocols. This low overhead frees up memory and processing power for other applications within the host processor.

The two IC suppliers have developed a number of tools to assist design-

ers in adopting their chips. These include application circuit reviews, a developer's kit and reference design (Fig. 4), Internet-based technical support, a bill of materials (BOM) and target pricing for a complete system, and flexible licensing strategies for the use of the hardware intellectual property (IP). California Eastern Laboratories, 4590 Patrick Henry Dr., Santa Clara, CA 95054; (408) 988-3500, FAX: (408) 988-0279, Internet: www.cel.com.

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