

**AN-PF-1007****Designing High Power GaAs FET Amplifiers  
Using Single Cell FET Parameters****INTRODUCTION**

Many different power GaAs FET die types are available from NEC. With the recent development of the NE430, NE345L, and the NE372 chips, some edification on proper matching techniques and considerations is in order. A method for developing matching circuits for thin film hybrid power amplifiers is given. While it is not the only method usable, it has proven to be a reliable approach. Circuit realization and material issues are also addressed.

Designing power FET matching circuits differs in approach from low noise amplifiers for a number of reasons. First, the physical size of these power FET chips is large enough to require a distributed analysis. Because of their low impedances, it is difficult to measure and characterize these chips using conventional 50-ohm characteristic impedance network analyzers. Secondly, even if a "perfect" distribution network were available to characterize an 8-cell device such as the NE372800 in a 50-ohm system, a 40 dB coupler directivity of the network analyzer could induce as much as a 35 percent error in the measured impedance ( $R_{in} = .78$  ohms). Lastly, power devices operating in the large signal mode cannot be treated as linear elements where their small signal parameters are used directly for design. For these reasons, a different approach is used. A single cell of the power FET is characterized with little error in a 50-ohm system, small signal models are developed for the input and output of the device, and the small signal models are modified in conjunction with the devices' D. C. parameters such that a quasi-linear design approach may be used.

**DEVICE CHARACTERIZATION**

For purposes of device characterization, NEC processes single-cell chips of each device. These cells are diced and characterized individually for D. C. and R. F. parameters. This "unit cell" data is available for most power FET device

series. The cells are analyzed for  $I_{DSS}$  and  $V_P$  after having been attached and bonded to a coplanar waveguide (CPW) test fixture. The devices are then biased to the desired operating conditions (usually  $I_{DSS}/2$ ) and characterized over a wide band on the HP8510 Network Analyzer. The calibration used is the in-fixture type employing open, short, and  $Z_0$  references. The data taken includes the bonding wires which may be deembedded later through the use of a microwave circuit analysis program. The wires used to bond the cells are usually fairly long (30 to 35 mils). This is because of the substrate layout, where the ends of the transmission lines (calibration reference planes) are considerably removed from the edges of the device. Figure 1 shows a chip mounted on a typical CPW carrier.

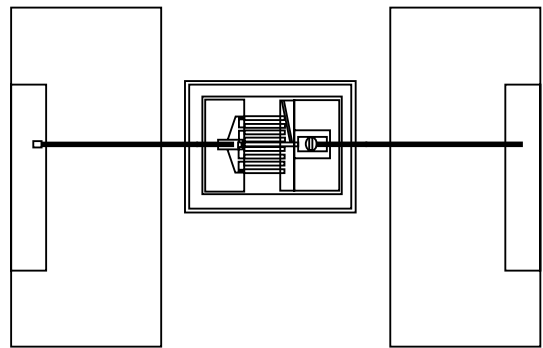


Figure 1: Power FET Cell on CPW Characterization Substrate

**MODEL DEVELOPMENT**

One-port models need to be developed for the input and output of the FET cell over the frequency band of interest. Assuming that a conjugate match is to be presented to the FET

input in the final circuit, the conjugate of  $S_{11}$  is presented to the input of the device. In this way, the effects of conjugately matching the input are approximately accounted for when determining the output model. The resulting values ( $S'_{22}$ ) are used to determine the one-port small signal output model as shown in Figure 2.

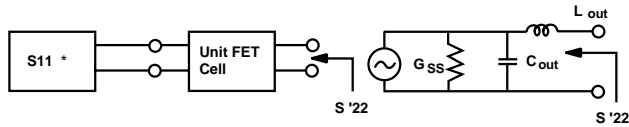


Figure 2: Modeling Output of FET

Next, the method outlined by Steve Cripps<sup>1</sup> is used to determine the optimum output conductance from the D. C. measurements:

$$G_{opt} = I_{DSS} / (2 * V_{DS})$$

The desired load conductance is then found as:

$$G_{Lopt} = G_{opt} - G_{SS}$$

where  $G_{SS}$  is the model conductance found from the small signal linear output model. The value for  $G_{opt}$  is used along with the reactive components determined in the small signal model to construct the “optimum” model as shown in Figure 3. The extent to which the value of output conductance varies from the small signal model to the “optimum” model is attributed to the differences between small signal and large signal operation. Output matching is then effected by matching from the system characteristic impedance to this model over the band of interest; i.e., a filter is designed to absorb the parasitics of the optimum model and transform from the system characteristic impedance to  $1/G_{Lopt}$  (Figure 4). These are the conditions under which maximum power transfer will occur for large signal operation.

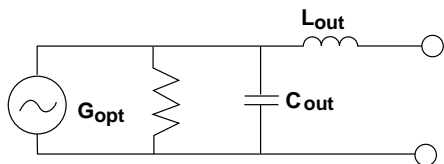


Figure 3: Optimum Output Model for Large Signal Operation

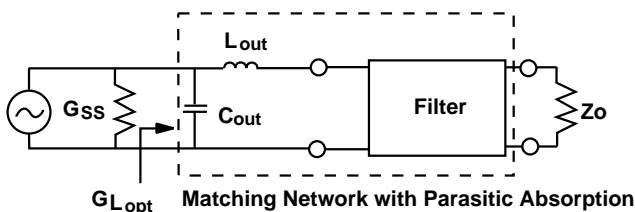


Figure 4: Optimum Output Load for Maximum Power Transfer

To determine the one port input model, the bilateral effects of the device are approximately accounted for by terminating the output in the negative image of the optimum output model<sup>2</sup>. In this case, the input reflection coefficient is defined as  $S'_{11}$ . The input model is then a simple series RLC network whose element values are tailored to fit the  $S'_{11}$  data obtained (Figure 5).

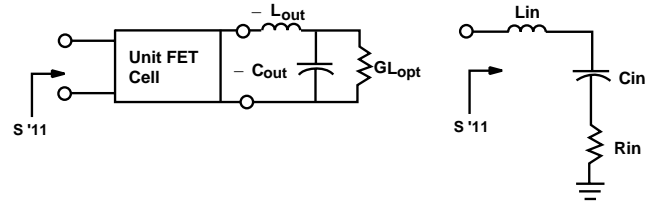


Figure 5: Determining Input Model

This procedure may be reiterated if desired; the deviation of the values obtained in each cycle from the final values is directly determined by the isolation of the device; i.e., the extent to which the device is unilateral. The model values for a design using the NE372100 were seen to converge to within a few percent of their final values after the first iteration.

**DESIGN APPROACH**

Input matching is accomplished by first resonating the bond wire with the input model capacitance at the center of the band. The real impedance is then transformed up to a higher value using another LC ladder section as shown in Figure 6. The values for these latter two elements are optimized to maintain the highest possible real impedance transform over the band of interest. Given  $L_T$ , the value for  $C_T$  may be found at  $f_0$ , the center frequency of the band:

$$C_T = 1 / [(2 * \pi * f_0)^2 * L_T * (1 + \{Rin / (2 * \pi * f_0 * L_T)\}^2)]$$

The device combined with these elements becomes the building block: a FET cell transformed to a real impedance over the band of interest.

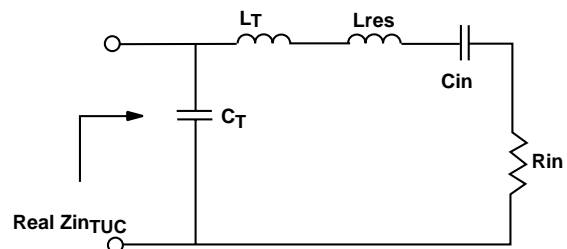


Figure 6: Real Impedance Transform: The Transformed Unit Cell

The size of the actual chip being used now comes into play. These transformed unit cells must be combined effectively and transformed into the final system characteristic impedance. The approach used is to parallel combine a number of

these transformed unit cells, and transform the resulting real impedance up in value using transmission line sections which are of quarter wavelength at mid band (Figure 7). In the diagram, the value of impedance after combining “n” parallel transformed unit cells is  $Z_{in\_TUC}/n$ . The quarter wave section is chosen with  $Z_T = (Z_{TC} * Z_{in\_TUC}/n)^{1/2}$  where  $Z_{TC}$  is the desired impedance level at the left hand side of the quarter wave section. These quarter wave lines are in turn parallel combined to give the desired system characteristic impedance. The number of transformed unit cells which may be combined is dependent upon a number of factors, including bandwidth, the maximum transform available from the quarter wave section, and size of the device, which will dictate the physical realization of the circuit. For example, performing 8 individual transformations on an 8-cell device is impractical because of the difficulty in realizing 8 separate transforming circuits in a limited amount of space. Also, if 8 quarter wave lines could be combined in parallel to 50 ohms, the impedance level at the end of each quarter wave would need to be 400 ohms. This would require quarter wave sections of characteristic impedance greater than 100 ohms, which are not easily or repeatably fabricated on alumina substrates. For an eight cell device, grouping 4 transformed unit cells together and transforming the resulting impedance up to 100 ohms has proven a viable approach. Values for the lumped elements and transmission line characteristic impedances may be optimized for best in-band VSWR.

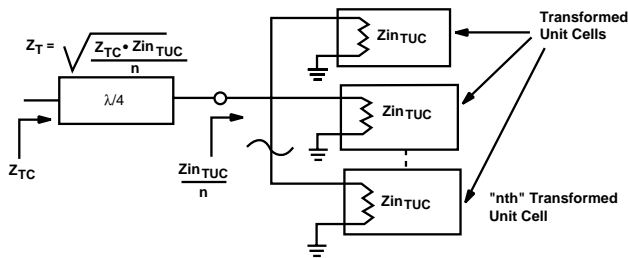


Figure 7: Combining and Transforming the Transformed Unit Cells

Output matching may be performed in a similar fashion; however, because the topology of the output model (Figure 3) is already in a lowpass form, the approach is to synthesize a lowpass filter which absorbs both the capacitive and bonding parasitics of the model. Depending upon the magnitude of the transform, it may not be necessary to use the same quarter wave techniques to transform the impedance up as were used for the input matching network synthesis. The method of combining adjacent sections in parallel, however, is the same as for the input circuit.

**REALIZATION**

With the topologies and element values chosen for input and output matching networks, the layouts are ready to be made. In doing this, some points needing consideration are noted below.

Materials used for the circuits depend upon the particular requirements of the amplifier. For most purposes, alumina may be employed. The quarter wave matching structures may become large, especially at low frequencies. However, if size is a concern, high-dielectric material may be used for either the entire circuit or portions of it. Such materials are available from Allied-Transtech (D8512 Barium Tetratitanate). For example, the value of the lumped capacitor for the input or output may, if small enough, be realized with a section of low impedance transmission line using a high dielectric substrate. In some cases, the whole circuit may be realized on high dielectric material. These approaches have been successfully implemented in X-band power amplifiers<sup>3,4</sup>. Another approach is to use special high dielectric capacitors which are manufactured with the same width as the multi-cell FET. Special values and sizes have been obtainable from American Technical Ceramics. In this case, caution must be used in choosing the appropriate value. Excellent discussions are available to aid in selection of capacitor types and materials for given applications<sup>5,6</sup>. Due to the distributed effects of the capacitor plates, the capacitor may be modeled as a lumped L-C network over the band of interest. First, the capacitor is broken up into  $2 * n$  sections (Figure 8), where “n” is the number of cells in the FET and “W” and “L” are in directions along the capacitor which are transverse and parallel to the signal path, respectively.

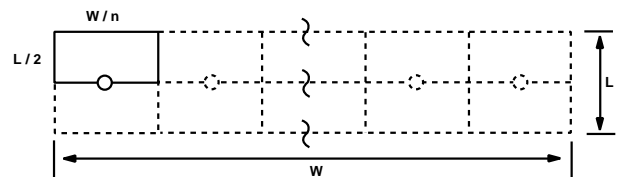


Figure 8: Partitioning of Discrete Capacitor for Distributed Analysis

In this analysis, the excitation is considered to occur at nodes along the line of symmetry of the capacitor as shown. One of the sections (being “W”/”n” units wide and “L”/2 units long) is then modeled as shown in Figure 9.

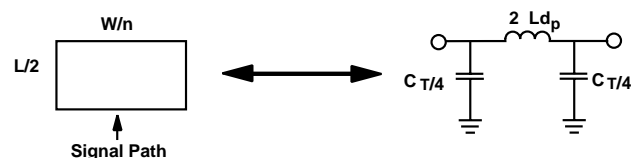


Figure 9: Modeling a Transmission Line Section by a C-L-C “Pi” Network

The substrate parameters used in the calculations are those of the capacitor dielectric. Assuming that the transmission line section is lossless, the value for  $2 * L_{dp}$  may be found<sup>7</sup> from:

$$2 * L_{dp} = Z_0 / (2 * \pi * f) * \sin (2 * \arctan (2 * \pi * f * Z_0 * C_T / 4))$$

where  $Z_0$  is the value of the characteristic impedance from the analysis of the transmission line section,  $C_T$  is the value

of the capacitor found in Figure 6, and  $f$  is the highest frequency in the band of interest. This model needs to be optimized to find the best fit. To model a section of the capacitor which is “ $W/n$ ” units wide and “ $L$ ” units long, two of these pi networks are then cascaded and reduced to the electrical equivalent as shown in Figure 10.

The capacitor next needs to be analyzed in the direction transverse to the signal flow. To do this, the section of transmission line having width “ $L$ ” and length “ $W/n$ ” as shown in Figure 11 is modeled as a tee network. The value of inductance is obtained from<sup>7</sup>:

$$L_{dt}/2 = Z_0/(2\pi f) \cdot \tan(\arcsin(2\pi f \cdot Z_0 \cdot C_T)/2)$$

As before, adjacent sections of the capacitor are cascaded and electrically reduced as shown in Figure 12. The values determined for  $L_{dt}$  are then used to bridge adjacent sections of the capacitor section model of Figure 10 to form the model for the entire capacitor of value  $C_T \cdot n$  and dimensions “ $W$ ” by “ $L$ ”. Figure 13 shows this model along with the nodes of excitation. With this model, analyses for even and odd excitation modes may be performed. It is seen that the values for  $L_{dp}$  affect the effective value of the capacitor significantly.

For example, for a capacitor with  $L = .020$ " and  $W = .076$ ", the effective value of a 3.5 pF capacitor is approximately 5 pF in X-band. Hence, the final value of capacitance used in the circuit may be expected to be considerably lower than the design value.

Another consideration in the layout is obtaining purely even mode excitation of the gate and drain pads. This is dependent on both the bonding to the device and the layout used. The bonding used must be as uniform as possible: all wires must have the closest possible match in length and profile. This may be controlled with either automated bonding or by using highly skilled operators. The other consideration is the layout. Steps may be taken to insure uniform phasing of the signals by using forked structures as shown in Figure 14. In this example, the circuit for the input matching network for the device transforms 4 parallel combined transformed unit cells up to 100 ohms, then two of these networks are parallel combined to result in a 50 ohm input impedance. The circuit appears small as it is realized entirely on high dielectric constant material. It is seen that the matching capacitor is uniformly fed by the forked structure. Each quarter wave transformer has been divided into two lines near the capacitor to further insure phase uniformity.

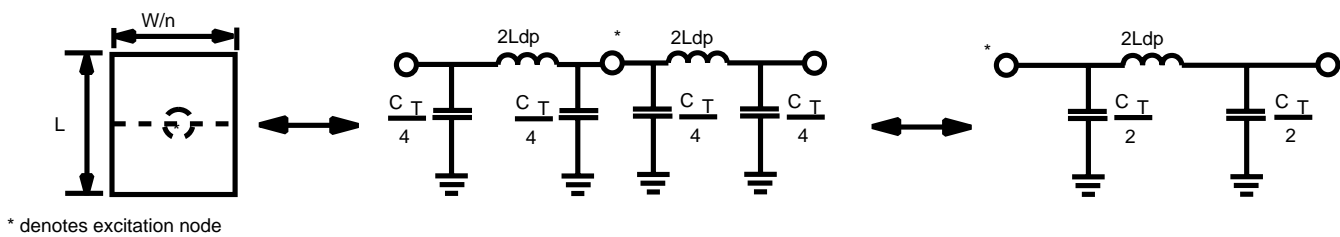


Figure 10: Model of Capacitor Section with Dimensions "W"/"n" x "L"

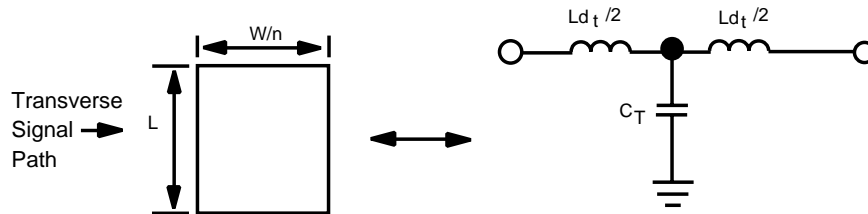


Figure 11: Modeling of Capacitor Section in Transverse Direction as L-C-L Tee

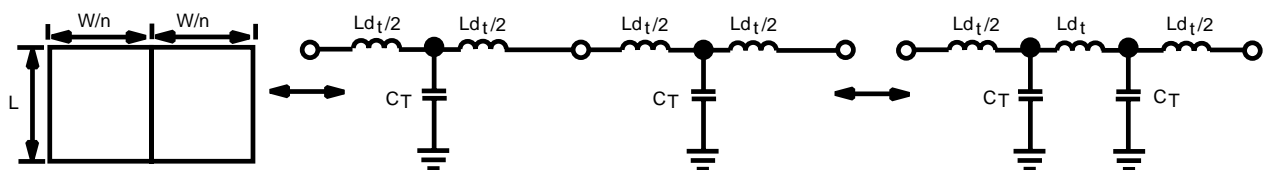


Figure 12: Cascading Adjacent Capacitor Sections in the Transverse Direction

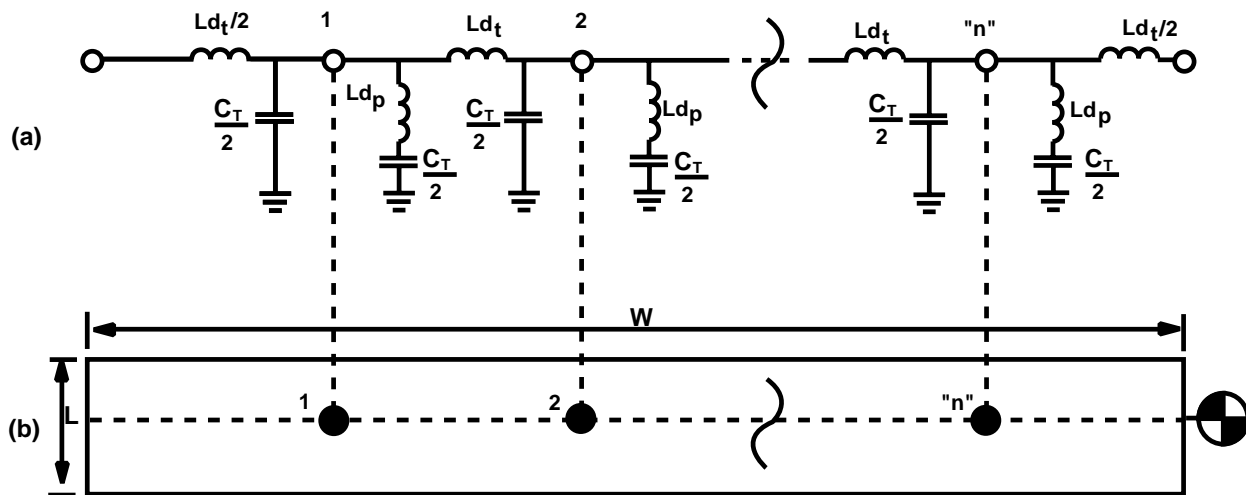


Figure 13 a: Lumped Model of Distributed Effects of Parallel Plate Capacitor  
 b: Excitation Scheme for Lumped Model (tap points of capacitors are numbered)

An analysis of the odd mode excitation of the inputs into the two quarter wave sections should also be undertaken, as the entire matching structure will behave as a ring resonator at the frequency at which the loop becomes an entire wavelength. For this reason, further restrictions must be placed on the thin film pattern and matching capacitor in order that this mode occurs significantly above the desired frequency band. Suppression of odd modes in the circuit may be accomplished by bridging the adjacent ends of the forks with thin film resistors. These transverse resistors serve to attenuate any odd modes which may occur.

Most of NEC's power FETs are manufactured with bottom side source metallization. The purposes of this metallization scheme are to minimize source to ground inductance and provide good heat dissipation. The source is connected to the back side of the FET using via holes, source wrap-around, or both methods. The FETs are manufactured very thin for low thermal resistance. It is very important to maintain a low thermal resistance path to the case. This requires that the material used for the carrier have high thermal conductivity. For the D8512 material, gold-plated copper carriers have been seen to work well, while Kovar (with slightly more thermal resistance) needs to be used for alumina circuits to prevent cracking due to thermal stresses. Figure 15 shows the profile view of a copper carrier developed for high relative dielectric material. The design utilizes discrete capacitors for both the input and output prematch. Note the different heights for each step. These heights guarantee that the circuit will be planar; i.e., that the tops of the substrates, capacitors, and FET will all be level with respect to each other. The carrier is plated with 100 microinches of nickel, then 100 microinches of gold.

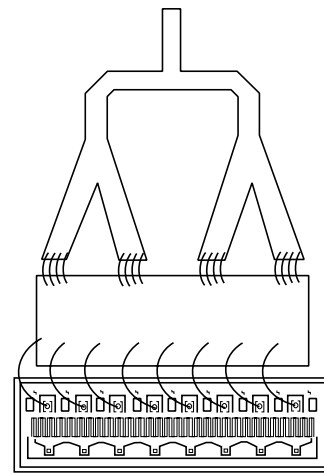


Figure 14: Forked Input Matching Structure

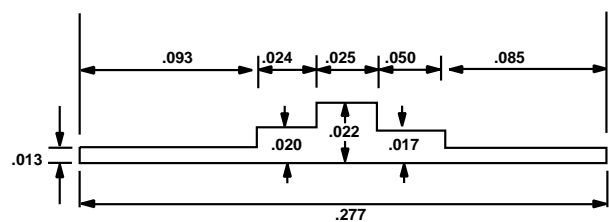


Figure 15: Profile View of Copper Carrier

A final consideration is biasing. Since the source will be grounded in most cases, both positive and negative supplies must be available. A gate supply may be implemented from a single positive supply, if desired, by using a method such as that shown in [8]. If on-circuit biasing is to be implemented, it may be done with a high impedance, quarter wave section of transmission line (stub) for fairly narrow bandwidths (20% or less). The main concern is making a line narrow enough to have a high characteristic impedance while

maintaining the current carrying capability necessary to bias the drain (in particular). This will depend on the FET being used. The bias needs to be injected at a low impedance point of the circuit, such as directly to the prematch capacitors. This helps diminish the effects of the off-resonance behavior of the stub.

## CONCLUSION

A proven method to design thin film hybrid power amplifiers using the single cell data available for most power GaAs FETs has been given. Material and circuit realization issues have been addressed.

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