

AN1043 Design of Power Amplifier Using the UPG2118K

I. Introduction

NEC's UPG2118K is a 3-stage 1.5W GaAs MMIC power amplifier that is usable from approximately 800 to 2500MHz. The UPG2118K is an excellent PA candidate for automatic meter reading, satellite uplink, and general short range wireless applications. It is fabricated with NEC's E-mode FET technology which eliminates the need of negative power supply and delivers high efficiency. Limited on-chip matching provides flexibility in both frequency selection and performance trade-off. In addition, the internal active bias circuits stabilize the drain quiescent currents over a wide temperature range as well as over the wafer-processing variation. The bias circuits can also be used for power control.

While the versatility of the UPG2118K makes it a good choice for many applications, for each particular application a certain amount of design work is required so as to fully utilize the device capability. This application note is intended to help UPG2118K users by providing, as a supplement to the data sheet, more detailed information on the internal circuitry as well as a practical design reference. Also presented in this application note (in the appendix) is the performance of two amplifiers designed with the UPG2118K for the respective applications at 915 MHz and 2.4 GHz.

II. Block Diagram

Fig. 1 shows a block diagram of the UPG2118K. The three gain stages are represented by transistors Q_1 , Q_3 and Q_4 . An additional transistor, Q_2 , which is cascoded with Q_1 , is used to reduce the RF leakage. Two inter-stage couplings are simply through capacitors, C_1 and C_2 . Although the values C_1 and C_2 were optimized for the GSM 1800/1900 applications, this simple coupling scheme allows usage at other frequency bands. A specially designed gate bias circuitry termed ABC (Automatic Bias Control) circuit is used to set the quiescent drain currents and to regulate the drain current against variations in temperature and wafer processing. There are two ABC circuits on this chip; one is for the control of the drain current of Q_3 while the other is for the first two stages. Input, output and interstage matching networks are required to achieve optimal performance, although the importance of these matching circuits to the overall performance varies.

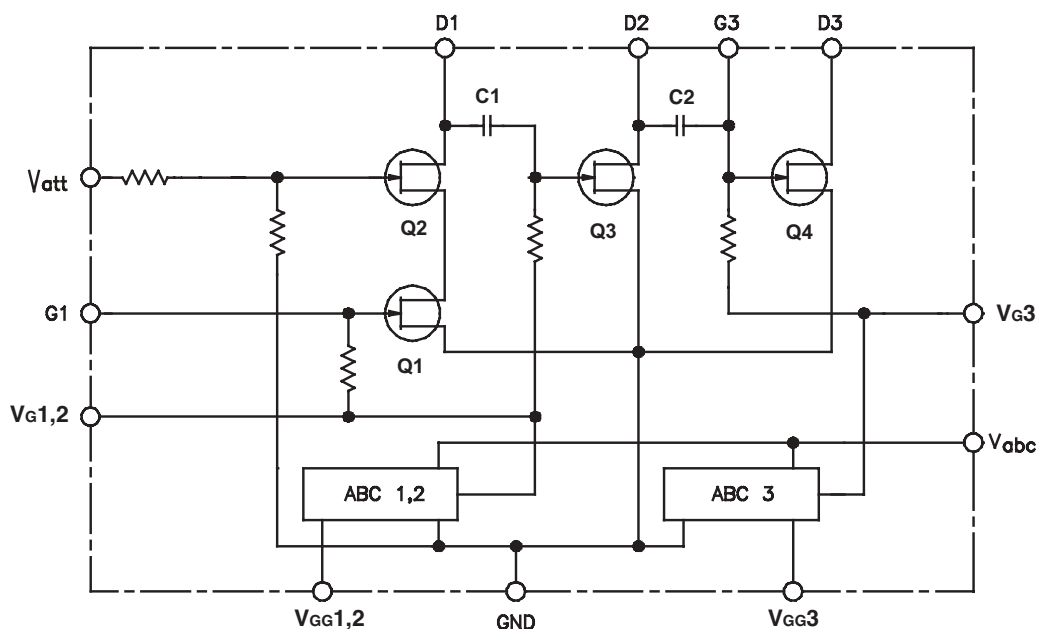


Figure 1. Block diagram of the uPG2118K

III. An Evaluation Circuit

To facilitate discussion, a 915 MHz application circuit is shown in Fig. 2 as an example. It is used here, however, mainly for demonstration purpose. The actual evaluation circuit board provided by CEL might be slightly different and the documentation provided along with the evaluation board presents the accurate circuit information.

Components used in this circuit are of generic type. Those microstrip transmission line sections that are part of matching circuit are given a component number (TL) and their electrical length and impedance are listed as well. These numbers are only estimated however, because the width of the actual traces is not uniform. The other PCB traces are merely for connection and are simply represented by solid lines.

For the convenience of circuit adjustment and evaluation of each individual stage, access to each pin on the chip, except for VG1,2 and VG3, is provided individually as shown in Fig. 2. For each DC line, including Vref1,2, Vref3, VD1, VD2, VD3, Vabc and Vatt, there are one or several shunt capacitors. Some of them (usually those with small capacitance values) are for matching purpose, which will be discussed later, the rest are bypass capacitors. In a real application circuit, where the layout of those DC lines will be surely different, the exact number, value and location of these bypass capacitors should be determined by the circuit designers according to their need.

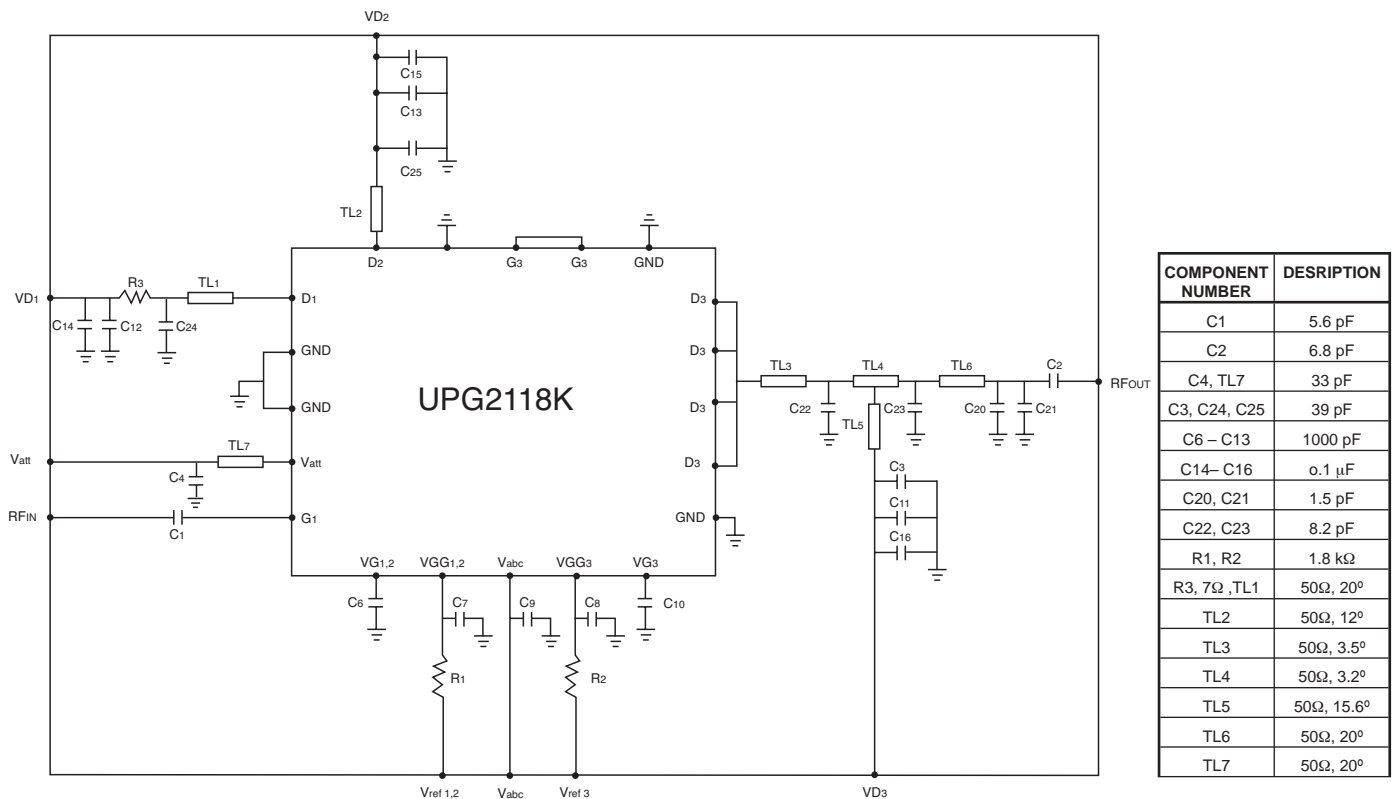


Figure 2. Schematic circuit of a 915 MHz evaluation board

IV. DC Bias Circuit

Both DC drain voltage and current can be adjusted over a relatively wide range for all three gain stages. Appropriate bias conditions are important to achieving the desired performance. While the DC drain voltages and currents of the FET's are directly supplied by external sources, the DC gate voltages, which control the drain currents, are supplied through two internal ABC circuits that in turn are biased through external components and sources.

The ABC circuit is a “current-mirror” based bias circuit. To end users, the main function of this circuit is to set and regulate the DC drain currents, although the actual circuit serves some other functions as well. For practical purpose, the function of the circuit can be represented by a simple diagram shown in Fig. 3. Like any current source that is based on “current-mirror” circuit, this ABC circuit has two basic features:

- i. The current to be controlled, I_D , is proportional to the reference current, I_{ref} ;
- ii. The stabilization of the controlled current is realized through R_{ref} which provides a negative feedback to the variation, and a higher value of R_{ref} makes the feedback more effective.

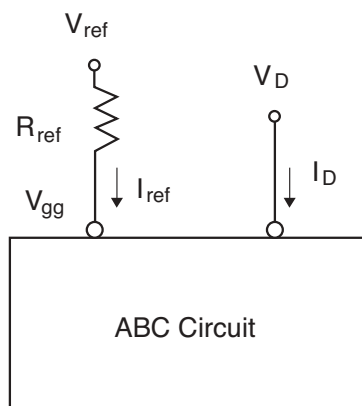


Figure 3. Diagram of the ABC Circuit

The quiescent drain currents of the UPG2118K are set by the combination of V_{ref} and R_{ref} . For each specific application, the optimal drain currents should be determined experimentally based on the specification requirement. In a practical design, the following procedure can be followed to determine the appropriate values for V_{ref} and R_{ref} .

- i. Choose the highest voltage that is conveniently available voltage on circuit board for V_{ref} . This is because for a given drain current a higher V_{ref} requires a higher R_{ref} which yields better stability against variations as mentioned previously. Designate this voltage as V_{r0} .
- ii. Since it is usually easier to change voltage than resistor on a prototype board, a fixed resistor value, designated as R_1 here, can be first used (the value used in the circuit in Fig. 2 can be a good initial choice). Then the drain current can be adjusted by changing the reference voltage with an external power supply. Once the desired current is determined, record the reference voltage and the voltage at V_{gg} pin, which will be designated as V_{r1} and V_{gg} respectively.
- iii. Using the following formula to calculate the new resistor value R_{ref} . This resistor value, when used with the desired reference voltage, V_{r0} , will set the quiescent drain current at the desired value.

$$R_{ref} = \frac{V_{r0} - V_{gg}}{V_{r1} - V_{gg}} \cdot R_1$$

V. Matching Circuits

As mentioned earlier, limited on-chip matching provides great flexibility in performance selection, but it also requires relatively extensive on-board tuning to achieve the desired performance. Generally, a prototype circuit board is recommended for the initial tuning and evaluation. The circuit designer can start the prototype circuit using one of the evaluation circuits provided by CEL. There are six ports where some tuning might be required. The following is a general guideline for the matching circuit at each port.

i. RF Input, pin “G1”

The importance of a matching circuit at this port is usually marginal. In Fig.2, no matching network other than a DC block capacitor is used. In some other cases a matching network consisting of a shunt capacitor and a section of microstrip line can improve both input return loss and overall gain. The S-parameter of this port, S_{11} , is in the range of a few -dB, depending on the frequency and

measurement power. Because the device has a peak in gain around 400MHz, the value of the DC block capacitor should be chosen as small as possible (in the few pF range) for the reduction of the gain at low frequencies.

ii. Gate of cascode stage, pin “Vatt”

For the stability reason this port should be well terminated by using shunt capacitor(s) (C4 in Fig. 2) to ground. The capacitor value and location have some impact on the RF performance too.

iii. 1st inter-stage, pin “D1”

This port is the drain bias line for the first stage. A tuning circuit with a shunt capacitor plus a small section of trace is recommended. For tuning, the user can first choose a shunt capacitor with high enough capacitance such that its impedance at the operating frequency, $1/\omega C$, is in the range of few ohms or lower, and then place it as closely as possible to the device without significant performance degradation. Such tuning circuit (which, in the case shown in Fig. 2, consist of C24 and TL1) essentially presents to the device a load that is transformed from an RF ground (at the location of C24) through a transmission line (TL1). This way the RF circuit is isolated from the rest DC circuit beyond the point of shunt capacitor. It is particularly beneficial when transferring the prototype circuit to the end product, in which some changes in the DC line layout and DC power supply are often unavoidable.

iv. 2nd inter-stage (pins “D2” and “G3”)

Pin “D2” is the drain bias line for the second stage and should be tuned in the same way described in section iii, paragraph. Pin “G3” is connected to the input of the last stage. At some frequencies and bias conditions a section of open trace which functions as a tuning stub helps improve the performance. But it is not always necessary. The designer can put an open section of trace at this port in the initial prototype circuit, particularly when the circuit board space is not extremely constraint, and observe its effect on the performance by gradually cutting the trace until finding the optimal length.

v. RF output (pin “D3”)

Impedance matching at this port is most critical to the ultimate circuit performance using this device. In fact the designer should first work on this stage to obtain a reasonably good performance and then do the fine tuning on the other ports.

As in any RF amplifier design using an FET transistor, the drain DC feed line needs to be determined first when the matching circuit is considered. A convenient and low cost solution for the DC line is a quarter wavelength transmission line. It not only provides a perfect isolation between the DC line and RF matching circuit at the fundamental frequency, but also provides a “short” at the second harmonic, which is often desirable for the better efficiency. Although a quarter wavelength transmission line is advantageous from the RF standpoint, it is impractical in some applications. In principle an inductor choke can be used in such cases to isolate the RF matching from the DC line. However the drain current of the uPG2118K reaches approximately 1A, which requires a relatively bulky and expensive inductor to avoid significant power dissipation and voltage drop across the inductor. As an alternative, a short section of trace plus a shunt capacitor might be employed as shown in Fig. 2 (TL5 and C3). For the same reason explained in the earlier section C3 should provide a good RF ground. This approach adds a little complexity to the design of impedance matching since now the DC line is part of matching circuit. But it is usually manageable.

The performance of the uPG2118K is strongly dependent on the output load impedance. The circuit can be optimized for one particular performance specification such as power, gain, efficiency and linearity or optimized for the best compromise among several specifications. In each case there is a corresponding optimal load impedance, which will be denoted as $Z_{opt} (= R_{opt} + jX_{opt})$. Conceptually, the function of the output matching circuit is to transform the terminal impedance, Z_{term} , which is usually, but not always, 50ohm, to Z_{opt} . For clarity, this concept and the associated terminology are illustrated in Fig. 4.

The optimal load impedances are not only bias and

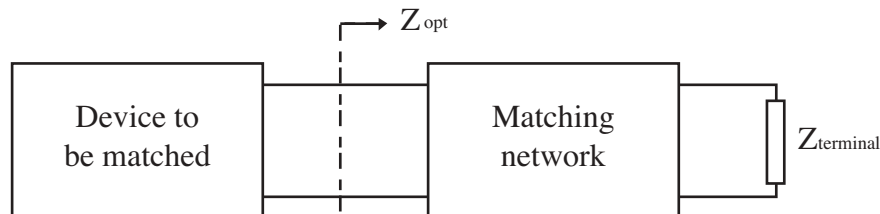


Fig. 4 Matching network from terminal impedance to optimal load impedance

frequency specific but also performance specific. Furthermore, even if an optimal impedance is given, an optimized performance is rarely achieved by simply implementing a matching network based on a Smith chart analysis – some bench tuning seems always unavoidable. For these reasons optimal impedances are not provided, instead, an approach that combines analysis/simulation and bench tuning is recommended and will be outlined as follows.

Like in most cases of a medium power (a few watts) device operating at a relatively low frequency (below a few GHz), an optimal load impedance of the uPG2118K consists of a resistive part of a few ohms and a small reactive part. The reactive part can be either inductive or capacitive, depending on the frequency and desired performance. The resistive part can be roughly estimated by a formula widely cited in the literatures on RF power amplifiers design (for example, Ref. 1):

$$R_{\text{opt}} = \frac{V_D^2}{2P_o}$$

here V_D is the drain voltage and P_o is the desired output power. For $V_D=3V$ and $P_o=31\text{dBm}$, which are typical for the uPG2118K, R_{opt} is around 4Ω . Once R_{opt} is known, a matching circuit that transforms Z_{term} to R_{opt} can be developed on a Smith chart or by some other means. For common values of Z_{term} , such as 50 or 75 ohm, a circuit topology of multiple sections of shunt capacitor and transmission lines is recommended. The output matching circuit shown in Fig. 2 is such an example. Since the intended operation frequency is in the range of 800MHz to 2400MHz, the total physical length of the transmission lines required for the appropriate matching is usually acceptable. When the circuit board space is tight, some tricks in layout routing can be employed. Multiple section matching topology usually works better as it provides more degrees of freedom in tuning.

Once a basic matching circuit is obtained, it might be beneficial, but optional, to perform a computer tuning of the circuit to observe the impedance movement on the Smith chart. This way, the designer can have some insight as to how the load impedance changes while performing the bench tuning. But a purely experimental approach should work just as well.

The last step in the design of matching circuit is bench tuning, which is almost always necessary to achieve an ultimately satisfactory performance. The performance of the uPG2118K is quite sensitive to the load impedance. The designer might find the initial performance to be considerably lower than what is expected (for instance, the output power can be a few dB too low). Usually it can be quickly improved once one or two key components are identified by experiment. It often, however, takes a

significant effort to achieve the last 0.5 dB improvement. This is particularly true when multiple performance specifications need to be balanced.

VI. Power control

Output power control of the uPG2118K is realized through three voltages: $V_{\text{ref}1,2}$, $V_{\text{ref}3}$ and V_{att} . When these voltages are used together, a maximum control dynamic range is achieved, when, on the other hand, only one or two voltages are used a less steep control curve can be achieved. Using multiple power supplies to control all three voltages can provide both maximum dynamic range and smaller control slope. Designers should determine the control scheme experimentally according to the requirements on the dynamic range, control slope and availability of the control voltages.

VII. Stability

It is not difficult to stabilize the circuit, nevertheless attention needs to be paid to the stability issue because the MMIC is not unconditionally stable over the entire frequency range. If the device oscillates, it usually occurs in the first cascoded stage. Appropriate terminations in the VD1 or/and Vatt line can always resolve the problem. In the circuit shown in Fig.2, R3 along with C12 and C14 (they are also used for the usual bypass purpose) on the VD1 line is such an exmple. A similar termination can be employed in Vatt line if necessary. Two 1000pF capacitors at G1,2 and G3 are recommended for better stability although not using them does not necessarily cause an oscillation.

Appendix

Performance Curves

Fig. 5 and 6 show the curves of Gain and PAE vs. Pin at 915MHz and 2.4GHz respectively. Fig. 7 shows the power control curve at 915MHz.

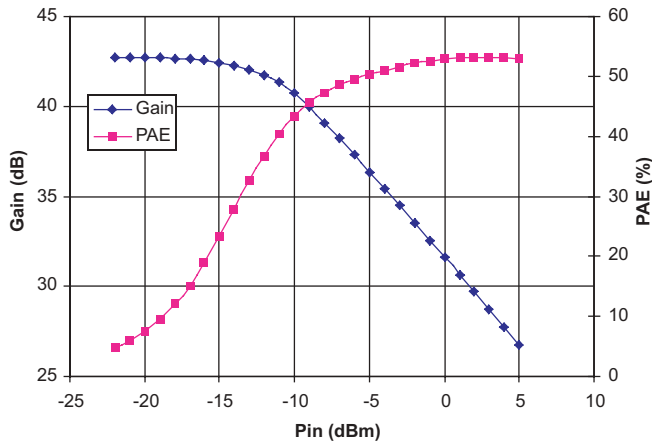


Fig. 5 Gain and PAE vs. Pin
915 MHz, VD1=VD2=VD3=Vabc=3.2V; Vref12=Vref3=Vatt=2.8V

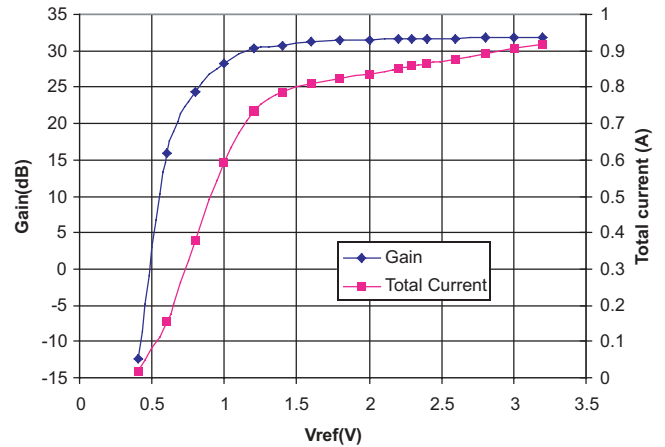


Fig. 7 Gain and Current vs. Vref @ 915 MHz
Pin=0 dBm, VD1=VD2=VD3=Vabc=3.2V; Vref12=Vref3=Vatt=2.8V

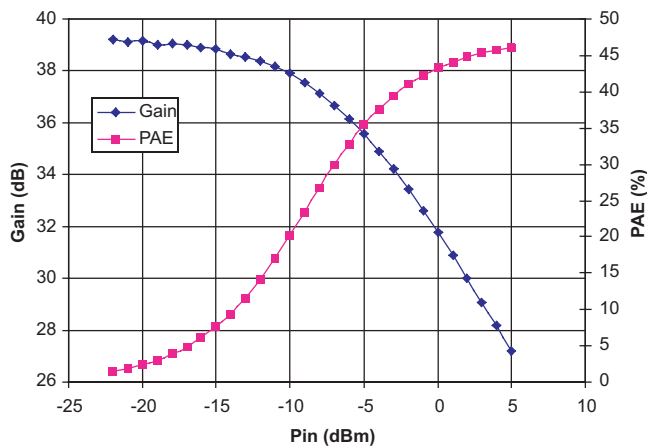


Fig. 6 Gain and PAE vs. Pin
2.4 GHz, VD1=VD2=VD3=Vabc=3.2V; Vref12=Vref3=Vatt=2.8V

Reference

1. M. Albulet, *RF Power Amplifiers*, Atlanta, Noble Publishing, 2001

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