

AN1039

Optimizing LNA Performance for CDMA Application Using Nonlinear Simulator

ABSTRACT

This application note will review the process by which designers can take advantage of the latest simulation tools such as **Xpedion's Design Systems** to achieve the optimal performance required by new digital communication system encryption including Code Division Multiple Access (CDMA).

Traditionally, for small signal amplifiers, there has been three distinct and generally incompatible basic design approaches that have met most design goals: the high gain, low return loss conjugately matched amplifier, the low noise amplifier and the high output power amplifier.

With the emergence of new technologies, in particular digital communications, the need for composite amplifiers that meet specific design goals not met by standard designs has increased. A previous article demonstrated how the different basic design types could be accomplished using a low cost NEC HJ-FET in a plastic package [1]. This article will emphasize improved performance of the original low noise amplifier for PCS by using series feedback techniques and predicting the system performance on the digital signal through nonlinear simulation analysis.

While the designs proposed may not yield the optimum design solutions for all PCS applications, it does introduce a few important RF and microwave techniques that can be applied to other digital applications.

CDMA DESIGN CONSIDERATIONS

CDMA uses correlative codes to distinguish one user from another within several channels, but in a much larger bandwidth per channel (1.25 MHz) than typical analog phone systems. These codes enable the superposition of several users within one channel and allow each user to operate in the presence of substantial interference. However, the proximity of high interference level signals to the users added to the continuous "on" state of the Power Amplifier (P.A.) on the transmit side dictate two of the main RF requirements of the subsystem: low noise figure and high linearity. These parameters are key in distinguishing other mobile application LNAs from a CDMA cellular receiver. The low noise figure ensures the appropriate carrier to noise ratio necessary to achieve the dynamic range required by the user, even after adding insertion loss from the input diplexer. The high linearity prevents distortion from outside of band signals such as the on board P.A. or second harmonics from the Amps band. Additionally, because the CDMA modulation scheme uses a diplexer to the antenna (as opposed to a switch turning either the transmit or receipt side on and off), the LNA needs to provide a fairly adequate input return loss to the diplexer or this component would be load-pulled. Unwanted pulling increases the diplexer's insertion loss and provides undesirable group delays in the received signal. With these system requirements in mind, the typical CDMA LNA is specified as per **Table 1**. As was explained in Reference [1], such requirements represent a composite design that cannot readily be conceived with traditional matching methods. Rather, with a state-of-the-art nonlinear simulator, engineers can quickly analyze the effect of series inductive feedback on their digital systems and synthesize an amplifier that will meet the system's requirements.

ITEM	PARAMETERS LNA SECTION	SPECIFICATIONS	SIMULATION RESULTS	TEST RESULTS	UNITS	NOTES
1	Operating Voltage	3	3	3	V	Low Voltage
2	Current	20	20	20	mA	Medium Current
3	Operating Frequency	1930-1990	1930-1990	1930-1990	MHz	IS-95 Cellular Band
4	Gain	13	15.5	14	dB	
5	NF	1.0	0.5	0.6	dB	
6	Input IP3	10	13	12	dBm	
7	Input VSWR (50 OHMS)	2:1 (-9.5 dB)	-10	-10	dB	
8	Output VSWR (50 OHMS)	1.5:1 (-14 dB)	-16	-16	dB	
9	Operating Temperature	-40 to +80	Not Stimulated	-40 to +80	°C	

Table 1. CDMA Low Noise Amplifier: Specifications, simulation and test results.

DEVICE CHOICE AND CHARACTERISTICS

Designers of high volume commercial products share common goals: high performance, small size, low costs and high manufacturing yields. When choosing an amplifier device, the choices are many: Silicon Bipolar Transistors, Si MOSFETs, GaAs FETs and more recently Heterojunction Bipolar Transistors (HBTs) [1]. The device chosen for this design is the [NE38018](#), a low noise, low cost Gallium Arsenide Hetero-Junction Field Effect Transistor (HJ-FET) housed in a miniature (SOT-343) plastic surface mount package. The device was selected because it offers an excellent compromise between cost and the high performance associated with High Electron Mobility Transistors. It provides Low Noise figure (0.55 dB), high transconductance gain (16 dB typical) and high linearity (output IP3 of 26 dBm typical) at 2 GHz, under reasonable bias conditions (2V, 20 mA). This usually is a prime concern for products in the mobile communication industry.

With a $0.6\ \mu\text{m}$ by $800\ \mu\text{m}$ geometry, the device is large enough to provide a reasonably high output power while providing a noise performance optimized for the 1 to 3 GHz bands. Additionally, the geometry, larger than other HJ-FETs makes it easier to design at the PCS and MMDS frequency bands both for impedance matching and stability. Other devices available to designers such as standard MESFETs (Metal Semiconductor Field Effect Transistors) or Silicon Bipolars were discarded because they provide a typical noise figure of 1.0 dB at 2 GHz. This leaves little margin for matching network losses and device variations when compared to typical PCS amplifier design goals. Other devices, such as smaller topology PHEMTs (Pseudomorphic High Electron Mobility Transistor) have the required low noise (0.3 dB at 3 GHz), but their small geometry ($0.15\ \mu\text{m}$ by $180\ \mu\text{m}$) does not provide the necessary output power. Additionally, most of these PHEMTs are prone to instability problems at low frequencies.

DEVICE NONLINEAR MODEL COMPARISON

The output of a nonlinear simulation is only as good as the nonlinear model that was used and the implementation of the model's equations within the simulator core engine. California Eastern Labs develops its own nonlinear models based on its internal device characterization and using an appropriate model within those that are commonly available in commercial simulators [2]. The model is then verified in different simulators and compared to the original data upon which it was developed.

The choice of a nonlinear model for a FET is determined by evaluating the DC characteristics of the device and comparing these measured characteristics to the characteristics of the nonlinear models. Different models implement the DC I-V curve equations differently [2]. For the device under consideration, NEC's [NE38018](#), Triquint's Own Model (TOM) best represents the P-HEMT, showing almost linear increase in drain current with increasing drain voltage at lower gate

voltages (**Figure 1**).

Once the DC model is verified, a good fit to the AC data can be achieved by adding the bond wire and package parasitic effects.

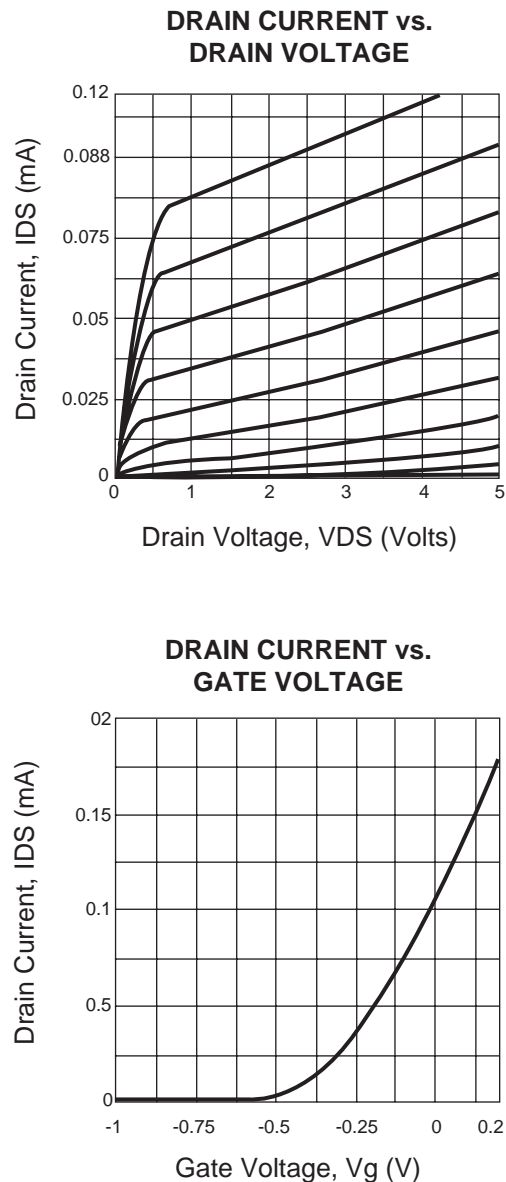


Figure 1. NEC NE38018 DC modeled.

DEVICE MODEL EXTRACTION RESULTS

The nonlinear device model for the [NE38018](#) was extracted by CEL and optimized using Xpedion Design System over the following ranges:

- DC: $V_{DS} = 0\ \text{V}$ to $5\ \text{V}$, $V_{GS} = 0\ \text{V}$ to $-0.8\ \text{V}$
- AC: $V_{DS} = 2\ \text{V}$ to $3\ \text{V}$, $I_{DS} = 10\ \text{mA}$ to $40\ \text{mA}$,
Frequency, $f_0 = 0.1\ \text{GHz}$ to $6\ \text{GHz}$
- Power: $V_{DS} = 3\ \text{V}$, $I_{DS} = 20\ \text{mA}$, $f_0 = 2\ \text{GHz}$

Figure 2. presents the topology and parameters of the device model and **Figures 3. -6.** compare the results of the extracted device model to the measured data. S-parameter comparisons (**Figures 3. -6.**) are shown at the desired LNA bias of $V_{ds}=3V$, $I_{ds}=20mA$ using Xpedion's post-processing interface. **Figure 7** shows the measured and modeled output power curves. The good agreement obtained based on these parameters verifies the accuracy of the nonlinear model and the appropriate

implementation of the model within the simulator. This is especially crucial for the noise performance, since the implementation of the noise parameters is simulator dependent and will vary to some extent depending on the simulator engine utilized. With the model verification completed, the designer can safely proceed to the LNA design.

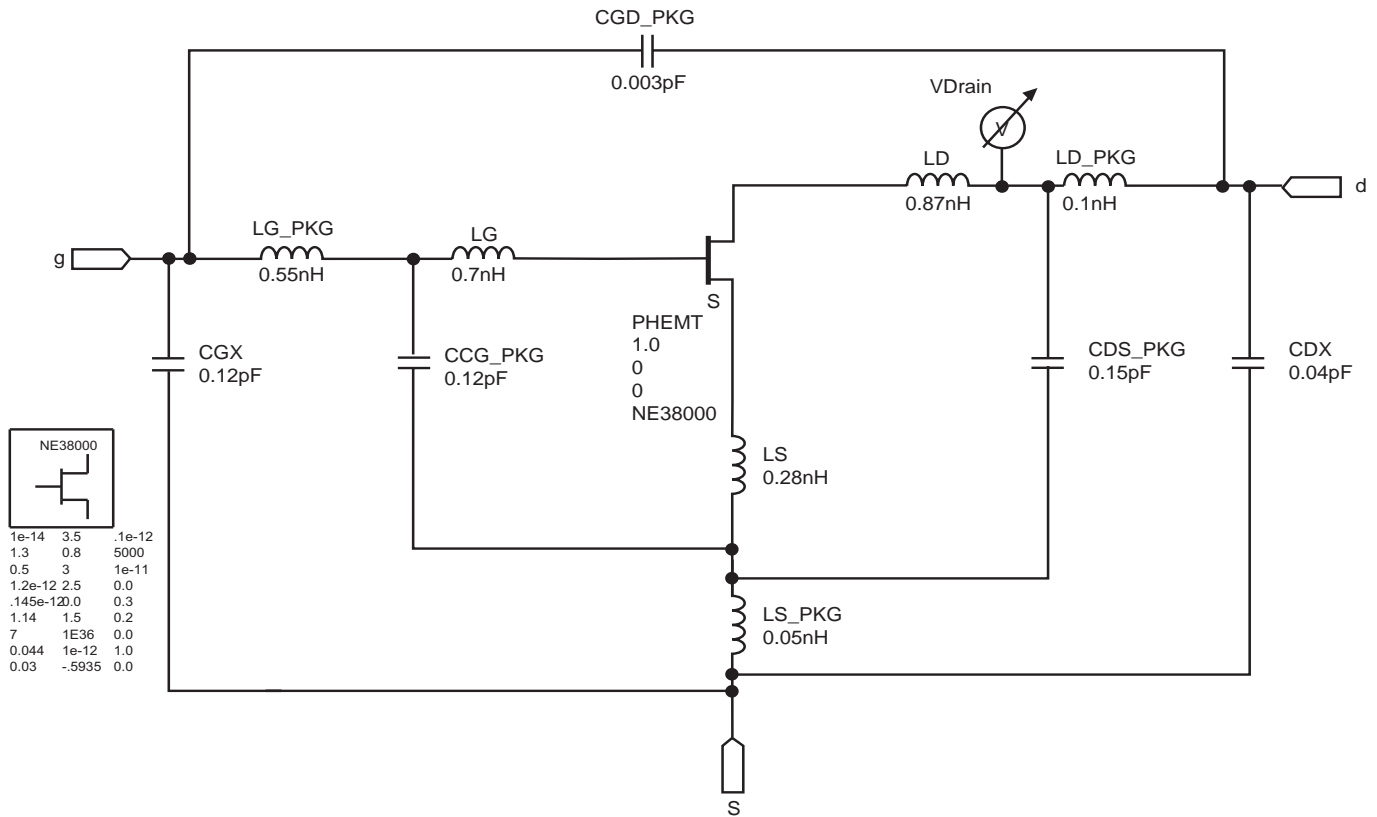


Figure 2. NEC NE38018 Nonlinear Schematic.

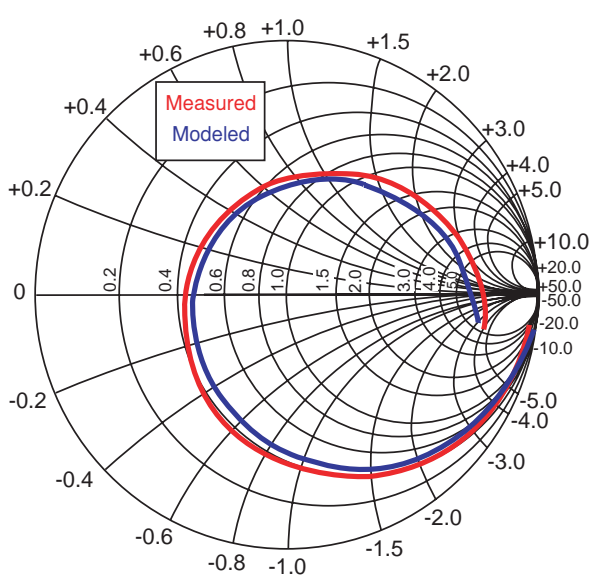


Figure 3. NEC NE38018 Measured vs. Modeled S11

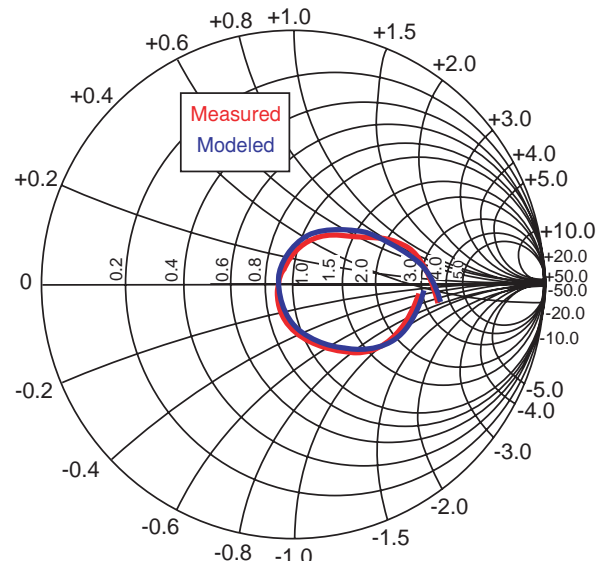


Figure 4. NEC NE38018 Measured vs. Modeled S22

POWER GAIN vs. FREQUENCY

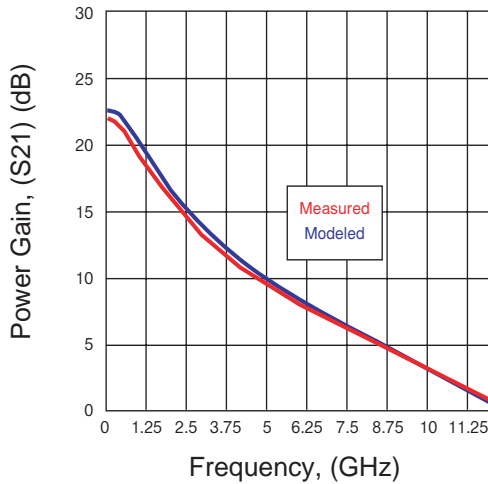


Figure 5. NEC NE38018 Measured vs. Modeled S21

ISOLATION vs. FREQUENCY

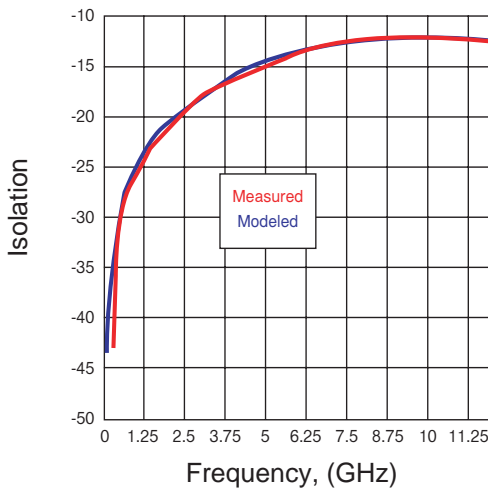


Figure 6. NEC NE38018 Measured vs. Modeled S12

POUT vs. INPUT POWER

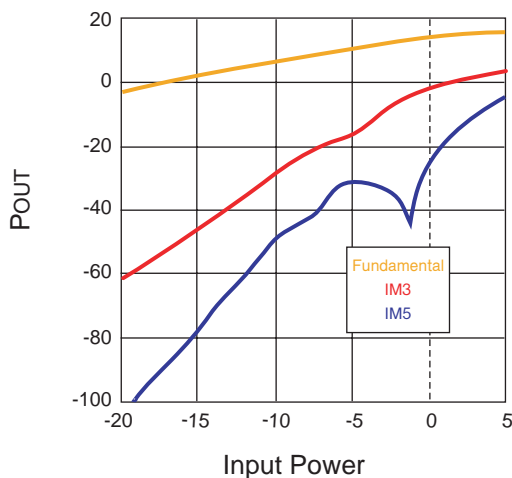


Figure 7. NEC NE38018 Modeled Output Power, IM3, IM5

LNA DESIGN

In this article, the design is for a 58 MHz bandwidth amplifier at a central frequency $F_c = 1960$ MHz. The bandwidth represents less than 3% of F_c and consideration will only be given to narrow band amplifier reactively matched designs (defined as less than 10% of F_c). As discussed earlier, there are three basic transistor amplifier designs available to engineers: maximum gain amplifiers, low noise amplifiers and high output power amplification. If design engineers can apply different matching networks on the input and the output to achieve their specifications (for example, power and noise figure), with hope of limited mutual effects, such an approach cannot be used when one tries to achieve both return loss and minimum noise figure at the same time. This is because the impedance that minimized the noise figure (Γ_{opt} the conjugate impedance to the ratio of the input voltage and current noise sources of the FET), is different from the Γ_{sm} (Gamma Source Match) that minimizes the return loss (Figure 8). So in practice, designers can only achieve good noise figure at the expense of the input match (NF_{min} of 0.6 dB for a R.L of -4 dB) or vice versa (a R.L of -20 dB with a NF_{min} of 1.6 dB)[1]

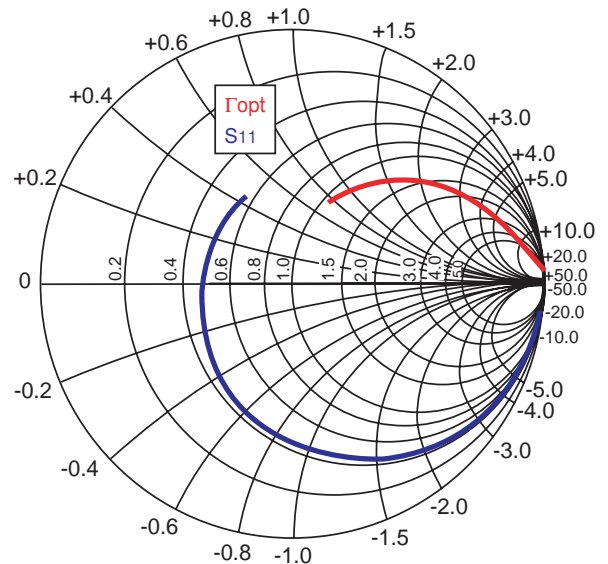


Figure 8. NEC NE38018 Gamma Opt and S_{11}

INDUCTIVE FEEDBACK CONSIDERATIONS

To achieve a respectable return loss while keeping the lowest noise figure, the designer somehow needs to bring Γ_{opt} close to Γ_{sm} or vice versa. This can be achieved by introducing inductive feedback on the source of the active device. As can be seen in Figure 9, increasing the source inductance from close to 0 nH (the minimum inductance provided by the source via hole) to 1.8 nH, brings the input S-Parameter S_{11} towards the center of the Smith chart, while having minimum impact on the noise match (noise circles).

A thin, 10 mils (0.254 mm) wide transmission line is used as the shunt inductance to ground. It is in general impractical to use a lumped inductance in the 0.4 to 0.8 nH range. Such inductance surely would have inductive parasitics at these frequencies that would exceed the desired value and tolerance variations in production would provide an unacceptable attrition rate. Evidently, this is one area that has to rely solely on simulation results as experiencing with transmission line lengths in a laboratory is not an available option. In this design, a 10 mils wide by 70 mils long line on each of the device's source pins provides the 0.7 nH inductance that provides the optimal performance.

Figure 10 exhibits how the source inductance modifies the performance of the device at 1,900 MHz: Noise Figure improves by a small margin (0.02 dB), and stability improves as well, allowing the engineer to use conjugate matching theory (since $K > 1$). An additional non-negligible benefit is the improved linearity that results: OIP3 improves by up to 6 dB when a few nHs are added to the source. However, the tradeoff is exercised on gain, which can potentially drop by 5 or 6 dB. In the design, the 70 mils long line corresponds to 1.778 mm which reduces the gain by 2.5 dB but increase OIP3 by the same amount. Upon completion of the design, the engineer can expect up to 5 dB improvement in IIP3. This variation is verified in **Figure 11**, where a lower gain accounts for the different curves, however, P1dB and PSat are mostly independent of Ls.

An additional inherent danger of this technique is the increased instability of the design at higher frequencies. As the frequency increases, the transmission line becomes relatively more inductive and increases the amount of feedback to the device's source up to an oscillation level. This issue can be reduced by carefully choosing the input/output matching topology so that transducer gain is limited at the frequency of potential oscillation. Design of a high-pass / low-pass matching network on the input and output is one solution that addresses the problem.

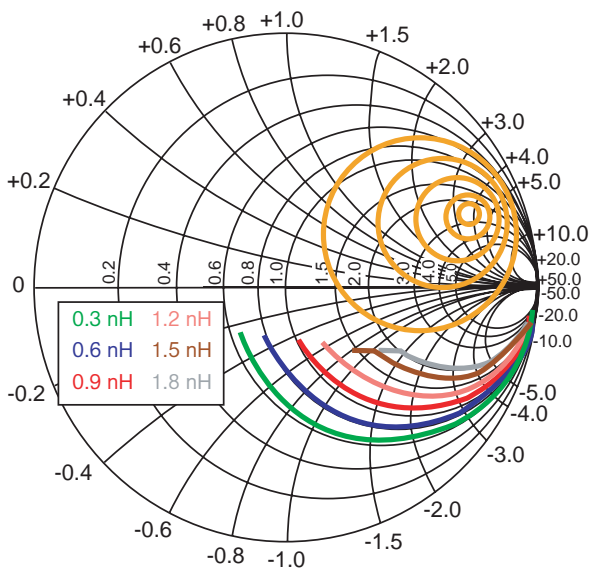
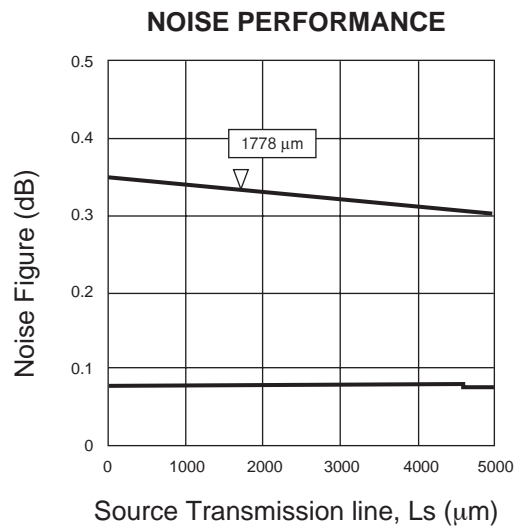
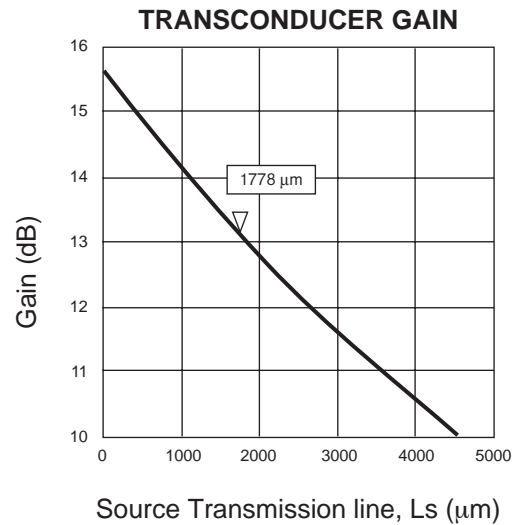


Figure 9. NEC NE38018 S11 and Noise Circles vs. Source Inductance



STABILITY FACTOR (K) at 1900 MHz

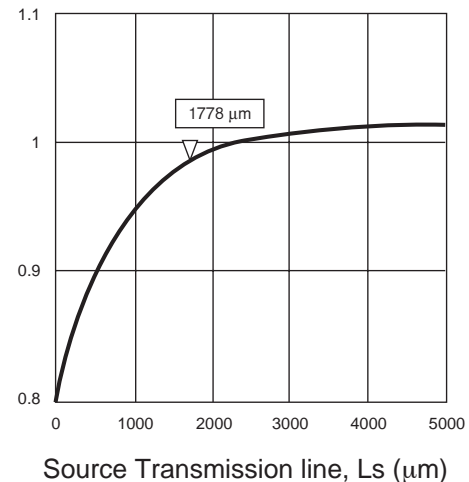


Figure 10. NEC NE38018 Noise Parameters (NFmin, Gain, Stability Factor and output Intercept) as function of source inductance Ls at 1900 MHz

SIMULATION RESULTS

LNA GAIN AND RETURN LOSSES

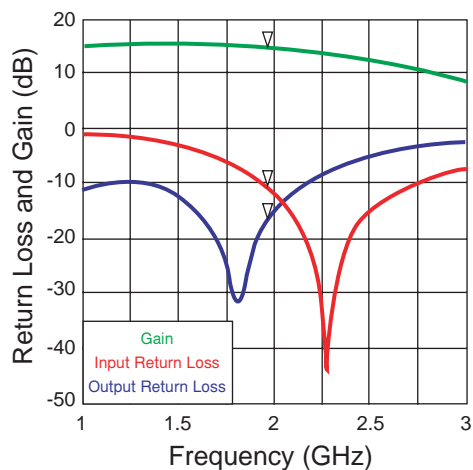


Figure 13. Simulated Input/Output Match and Gain.

LNA GAIN

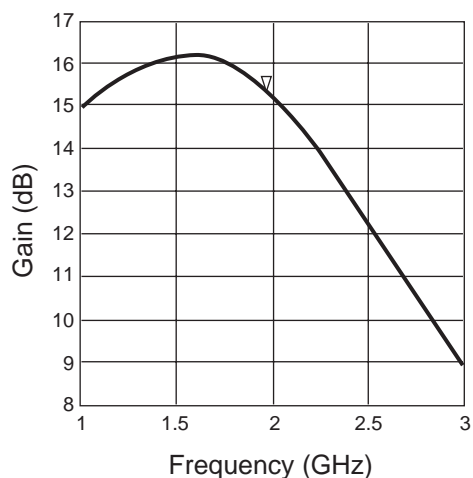


Figure 14. Simulated Gain Response

LNA NOISE PERFORMANCE

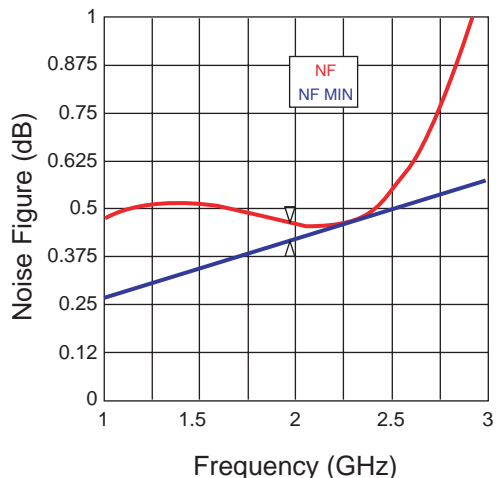


Figure 15. Simulated LNA Noise Figure and Optimum NFmin.

NONLINEAR CIRCUIT SIMULATION

INTERMODULATION AND OUTPUT POWER SIMULATION

Having achieved a good linear performance, design engineers can now take advantage of non-linear simulator features which use the Harmonic Balance and Envelope analysis to provide the nonlinear behavior of the design.

Envelope Analysis

The Adjacent Channel Power Ratio (ACPR) is the most critical parameter to simulate for the CDMA communication system because it is the only test that really reproduces the disrupting effect that a transmitted signal can have on other channels. It is important as it indicates how much power the receiver will transmit or generate outside its channel and thus how much it will interfere with adjacent channels. Proper simulation of the ACPR requires an input signal, which has the appropriate peak to average power ratio. In the CDMA encoding, this ratio depends on the particular active channels being used and is arbitrarily simulated using a time varying signal envelope superimposed on the RF input signal. This can provide a very accurate simulation of ACPR since true nonlinear and dynamic circuit behaviors (signal modulation of bias) are included. **Figure 17** shows the resulting spectra for two different input power levels and **Figure 18** the resulting output eye diagram under high ACPR conditions. However powerful these results may be, under Xpedion Design Systems, each simulation took less than 30s to complete on a 400 MHz PII laptop.

OUTPUT POWER SPECTRUM

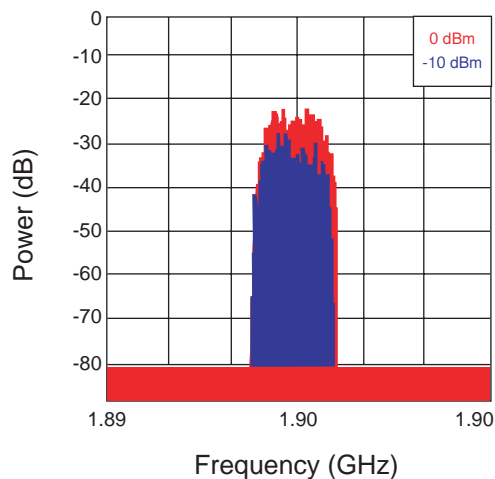


Figure 17. Spectral regrowth for Pin = -10 dBm and 0 dBm

OUTPUT VOLTAGE TONE

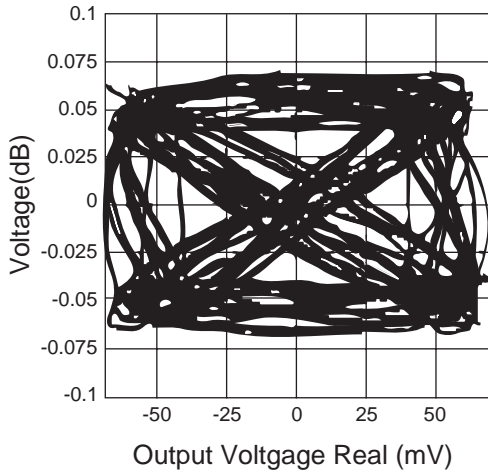


Figure 18. Output Eye Diagram(trajectories)

Circuit Testing

Upon achieving satisfying results with the simulation and choosing the appropriate circuit values for the different components, a prototype board was constructed and tested for compliance with the proposed specifications. The performance results are reported in Figure 20 – 22, summarized in Table 1 and are shown to provide a good agreement with the simulated results. The assembly drawing and billing of materials are displayed in Figure 19 and Table 2.

LABORATORY TEST RESULTS

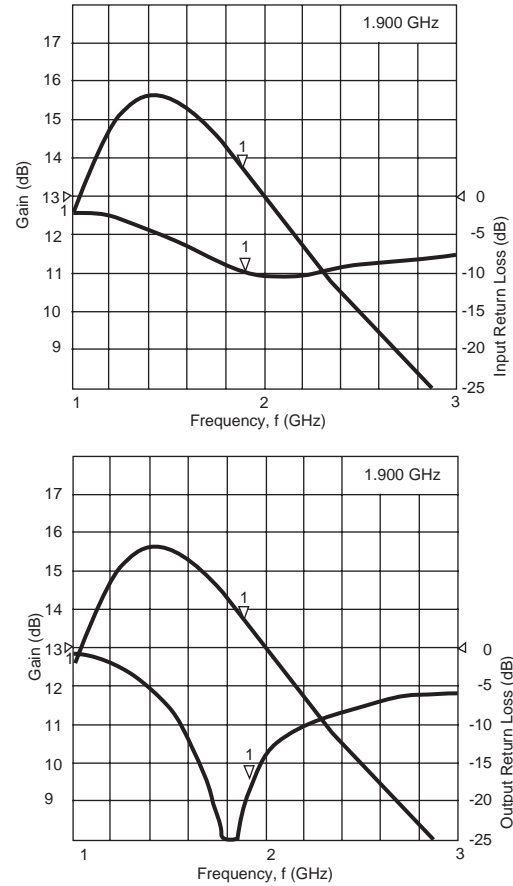


Figure 20. LNA Gain and Return Loss test results

NOTES: UNLESS OTHERWISE SPECIFIED.

CEC/NEC
LOW NOISE AMPLIFIER

QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	TF-100413	NE38018-EVAL TEST FIXTURE BLOCK		13
1	LL 1608-FHR10J	L1	100µH INDUCTOR TDKD	12
1	LL 1608-FH3N3S	L2	3.3µH INDUCTOR TDKD	11
1	LL 1608-FH5N6S	L3	5.6µH INDUCTOR TDKD	11
1	MCH185100JK	C1	0603 100pF CAP RDHM	10
1	MCH185A560JK	C4	0603 56pF CAP RDHM	9
1	MCH185A2R7CK	C3	0603 2.7pF CAP RDHM	8
1	MCH185A121JK	C5	0603 120pF CAP RDHM	7
2	MCH185C102KK	C2,C6	0603 1000pF CAP RDHM	6
2	B81-6116	C7,C8	4.7 µF CAP ALVK	5
1	NE38018	U1	IC NEC	4
3	2340-6111	P1	PIN HEADER 3M	3
2	2052-1215-00	J1,J2	DSM JACK OMNI SPECTRA	2
1	FD-100713	PCB	LOW NOISE AMPLIFIER FABRICATION DRAWING	1

APPROVALS	DATE	TITLE
DESIGNED	7/28/98	NE38018-EVAL ASSY DWG FOR CDMA APPLICATIONS, 1900 MHz
CHECKED		
PROJECT ENGINEER		
QUALITY		

CEC/CALIFORNIA EASTERN LABS
4350 PATRICK HENRY DR, SANTA CLARA, CA, 95054

SIZE: FROM NO. DWG NO. AD-100738
SCALE: 1:1 RELEASE DATE: NR SHEET 1 OF 1

Figure 19. NE38018 Evaluation Board Assembly

Reference Designator (Refer to Figure 11)	Description	Approximate cost in \$ (100K quantities)
U1	NE38018 GaAs HJ-FET microwave transistor (NEC)	0.40
C7, C8	4.7 mF SMT AVX capacitor	0.02
C2, C6	1000 pF SMT chip capacitor, 0603 package	0.02
C5	120 pF SMT chip capacitor, 0603 package	0.02
C3	2.7 pF SMT chip capacitor, 0603 package	0.02
C4	56 pF SMT chip capacitor, 0603 package	0.02
C1	10 pF SMT chip capacitor, 0603 package	0.02
R1 (2 in parallel)	56 KW chip resistor, 0603 package	0.005
L3	5.6 nH Inductor, TOKO	0.05
L2	3.3 nH Inductor, TOKO	0.05
L1	100 nH Inductor, TOKO	0.05
PCB1	0.031 thick double sided Getek printed circuit board	0.5
	Total parts cost (approximate)	\$2.53

Table 2. LNA Billing of Materials

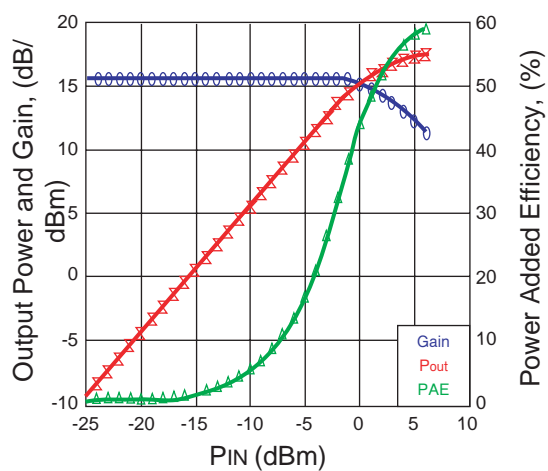


Figure 21. LNA Output Power Performance and Efficiency

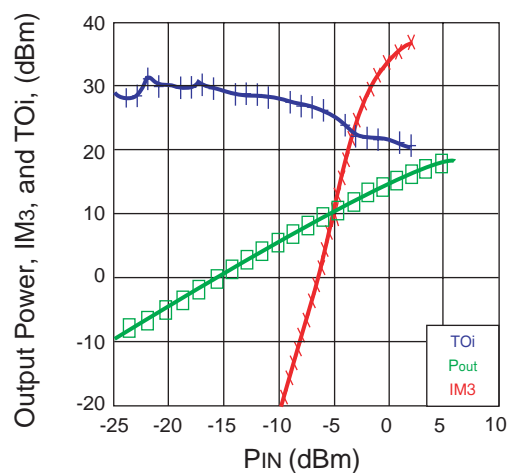


Figure 22. LNA Intermodulation Products Vs. Input Power

SUMMARY

This application note has demonstrated an LNA design at 1.9 GHz using one of NEC's new super low cost GaAs P-HEMTs which is optimized for mobile applications, especially those with a CDMA input signal. The required performance specifications were presented, simulated and tested. The inductive series feedback technique was described and the concept was demonstrated using *Xpedion's design suite*. *Xpedion's* simulation software was then used to predict and optimize the LNA performance in regards to gain, noise and ACPR performance. Finally, optimized measured results were reported and resulted in an LNA that met all the specification goals for a typical CDMA application.

By applying the design techniques presented in this applications note and understanding how inductive feedback affects different design parameters, engineers can quickly develop an LNA that is customized to their requirements. The use of powerful simulation tools such as *Xpedion's* design suite can only accelerate the design cycle by predicting the design's performance, optimizing circuit parameters to achieve the target goals and reducing on bench tuning. To further the robustness of their design and gain an invaluable insight into future manufacturing yields, designers can also take advantage of *Xpedion's* statistical analysis tools and statistically "center" their designs for minimum production attrition.

The NE38018 is an excellent choice for mobile communication LNAs because of good microwave performance at low power biasing, compact packaging, low cost and NEC's consistent processes. A very compact PCS LNA was presented that would cost just over \$.80 in 100K quantities for high volume manufacturing.

REFERENCES

- [1] California Eastern Laboratories, AN1022, "**Designing Low Noise Amplifiers for PCS Applications.**"
- [2] California Eastern Laboratories, AN1023, "**Converting GaAs FET Models for Different Nonlinear Simulators.**"
- [3] California Eastern Laboratories, AN1033, "**nonlinear HJ-FET Model Verification in a PCS Amplifier.**"

California Eastern Laboratories

Exclusive Agents for NEC RF, Microwave and Optoelectronic semiconductor products in the U.S. and Canada

4590 Patrick Henry Drive, Santa Clara, CA 95054-1817
Telephone 408-988-3500 • FAX 408-988-0279 • Telex 34/6393
Internet: <http://WWW.CEL.COM>

Information and data presented here is subject to change without notice. California Eastern Laboratories assumes no responsibility for the use of any circuits described herein and makes no representations or warranties, expressed or implied, that such circuits are free from patent infringement.