CEL California Eastern Laboratories

APPLICATION NOTE

AN1038
A 70-W S-Band Amplifier For MMDS & Wireless Data/Internet Applications

Shansong Song and Raymond Basset
California Eastern Laboratories, Inc
4590 Patrick Henry Drive
Santa Clara, CA 95054-1817

ABSTRACT

This paper describes a 70 W, 2.5-2.7 GHz balanced compact amplifier optimized for linearity. It uses a “Twin” GaAs MESFET NES2427P-60 device(1) designed for MMDS and Wireless Internet applications. It consists of two pairs of pre-matched chips mounted in one package. The amplifier was designed for linearity from the device optimum impedances for IMD3 performance. It exhibits the following typical performance in the 2.5-2.7 GHz instantaneous bandwidth: IMD3 of -45 dBc at 40 dBm output power each tone and has at 1 dB gain compression 12.7 dB of gain (G-1dB), 70 W of output power (P-1dB) and 40 % of power-added efficiency (PAE). The device is biased at Vds=10 V and Idsq=12 A.

INTRODUCTION

Multi-Point Multi-Channel Distribution System (MMDS) and Wireless Data/Internet technologies are the latest transport media for television broadcasting and internet. They require the use of reliable linear power amplifiers. In order to meet this requirement, a compact amplifier was designed based on device modeling and characterization with a two-tone signal for optimum IMD3 at a defined output power. The amplifier configuration was also an important issue that was considered to obtain good linearity, good stability, low circuit loss and good external matching. The development of this amplifier includes the modeling and characterization of the “Twin” GaAs MESFET device, NES2427P-60(1), used in this amplifier. This paper also presents the design methodology of the external input and output matching circuits of the GaAs device and a two-arm branch 90° coupler. The performance of this compact amplifier is presented and discussed.

DESIGN CONSIDERATIONS

Design Goals:

The goal was to design a compact linear power amplifier using a 60 W class A-B “Twin” device, NES2427P-60(1), that delivers a power of 40 dBm each tone with an IMD3 lower than -40 dBc in the 2.5-2.7 GHz instantaneous bandwidth. The requirement for G-1dB typical was 11.0 dB with a gain flatness better than +/-0.5 dB. The target for P-1dB typical was 48.0 dBm.

DESIGN CHALLENGES

The amplifier circuit optimization for linearity and the accurate prediction of the amplifier performance require an available device model and characterization for a two-tone signal. The device was modeled and characterized with a two-tone signal at a level of output power of 40 dBm each tone in the 2.4-2.7 GHz band.

The design challenge was to match the device optimum output impedance for IMD3 to a 50 ohm load in the 2.5-2.7 GHz bandwidth with an excellent return loss (better than 18 dB) and to minimize the loss of the output matching and combining circuit. The input circuit is not as critical as the output circuit since it does not significantly affect the output power of the amplifier. Its matching and loss have to be excellent only at the maximum frequency for gain consideration. Amplifier stability is always an issue with high power amplifiers. The splitter and the combiner have to be selected for high isolation (20dB), low loss (0.25 dB), good balance and ease of integrating to the amplifier layout. The choice of the amplifier configuration is also important if a good external match is needed to isolate the driver from the power stage.

MODELING & CHARACTERIZATION

The device used in this amplifier is a class A-B MESFET “Twin” device(1) which consists of two separated pairs of chips with their internal matching circuits mounted in the same package. The package has two gate and two drain connections without any internal connection between the two sides of the device. Such devices are sometime called improperly “Push-Pull” devices. The reason being is that this concept is coming from lower frequency applications HF, VHF & UHF using Si devices(2&3) with internal connections between the two sides of the device to take advantage of the virtual ground created by the push-pull configuration. The high power GaAs devices at L-band and higher frequencies do not have such internal connections(4). This is because their transversal dimensions are too large. In this case, these devices are not “Push-Pull” devices. They are devices with two identical sides called by CEL “Twin” devices. The configuration of the amplifier defines only how the devices operate. They can be combined the same ways as single-ended parts: in balanced configuration (90° hybrid), in push-pull configuration (baluns(4,5&6)), in phase combining (Wilkinson) etc.

To model such devices, only one side is considered. A simplenarrow band external input and output matching circuits with biasing circuits were designed. At each frequency, the input circuit was tuned for maximum return loss and the output circuit was optimized for IMD3. The performance, the source and load impedances were measured and recorded. These impedances are relatively high and do not present any difficulty to be measured with a good accuracy because the device is internally pre-matched.

The table 1 shows the half-device impedances versus frequency. In these conditions and for half the device, the following performance was obtained in the 2.5-2.7 GHz bandwidth: P-1dB=45.0 dBm, IMD3=-41 dBc to -43 dBc at 37 dBm each tone and G-1dB= 13.3dB.

In addition to the device characterization with a two-tone signal, the device was characterized with one-tone signal at 1 dB gain compression and its S-parameters were measured at small signal in the 1.5-3.5 GHz band. The S-parameters were used for gain and stability analysis at small signal.

Table 1 Optimal Input and Output Impedances

Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)
2.4	4.9	-9.1	17.2	16.4
2.5	4.0	-4.2	21.9	12.3
2.6	8.0	1.7	18.4	10.1
2.7	6.7	-2.4	16.8	11.1

The output circuit is optimized for IMD3 when the output power is 37dBm each tone for half the device.

AMPLIFIER DESIGN

Amplifier Configuration:

Contrary to popular belief, for bandwidth less than one octave there are no advantages in using a push-pull amplifier in terms of bandwidth and linearity. The disadvantages are:
* Low isolation between the two sides of the device if a classical balun is used (only 6dB)
* Poor external input and output match.

On the other hand, the balanced configuration has the same performance as the push-pull concerning bandwidth and linearity (bandwidth less than one octave) and has the following advantages:
* High isolation between the two sides of the device
* Good external match
* It is easy to design printed 90-degree splitters/combiners for marrow band applications that can be easily integrated with the layout of the amplifier
* Good reliability: the failure of one device side does not result in total failure: the output power drops by 6 dB.

For the above reasons the balanced solution was selected for this amplifier.

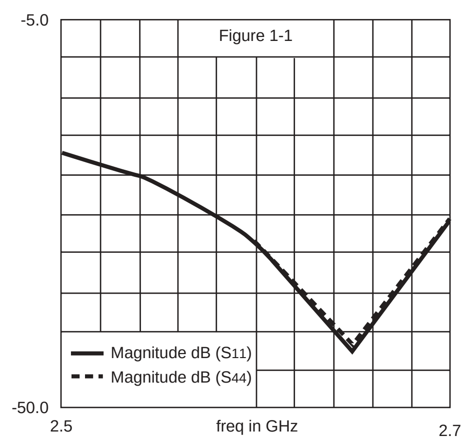
SPLITTER/COMBINER DESIGN:

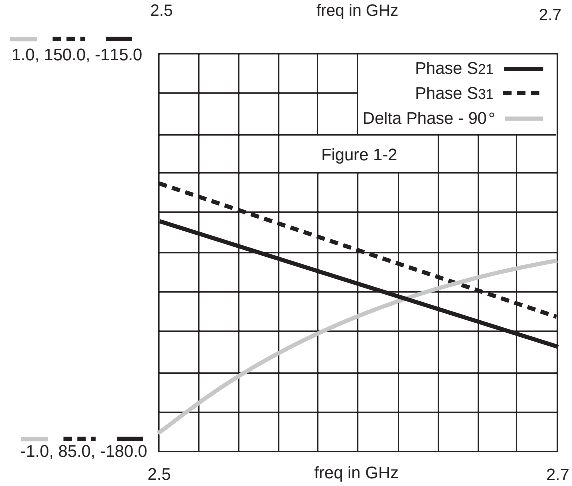
For balanced amplifiers, there are many kinds of couplers that can be used; such as Lange couplers, Wilkson with 90° phase jog on one port, two-arm branch 90° hybrid, etc. In this project, a two-arm branch 90° hybrid was selected due to its simple layout and ease in integrating with the amplifier layout. Since the input and output matching circuits realize the matching of the device to 50 ohm impedance, the hybrid does not perform any impedance transformation and all its port impedances are 50 ohms.

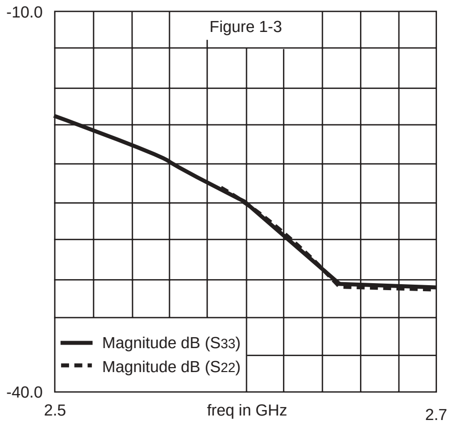
The design of the hybrid was performed with HP MDS software. Also HP MOMENTUM software was used to perform the EM simulation. The comparison of the simulated results between MDS and MOMENTUM software showed a slight difference in the coupler layout. The results from the MOMENTUM software were used for the coupler's final layout. The final EM simulation shows that this 90-degree hybrid has more than 20dB of isolation between its coupled ports and 20 dB of return loss for each port. Its balance is better than 0.1 dB in magnitude and 90+/-1° in phase. The figure 1-1 to Figure1-5 show the detailed simulation results.

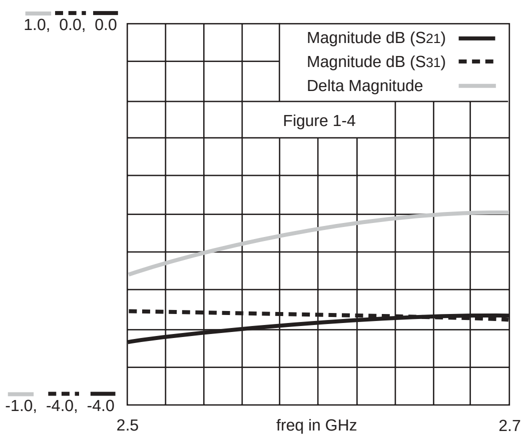
Figure 1-1 to 1-5 EM Simulation Results of Hybrid

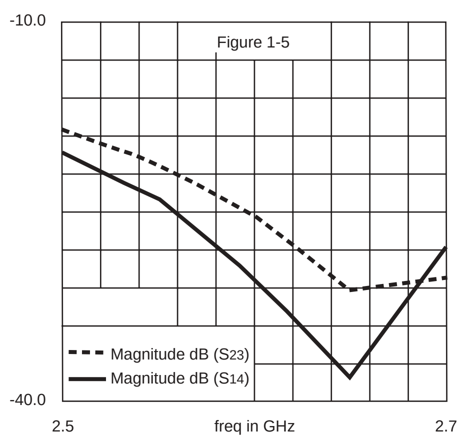
INPUT MATCHING CIRCUIT DESIGN











The input matching circuit was optimized for flat gain in the 2.4-2.7 GHz bandwidth and to have the best match to 50 ohm impedance at the highest frequency. It consists of two sections using only transmission lines with all the stubs being open stubs. In order to cover the 2.4 to 2.7 GHz bandwidth, sections with low Q were selected for the design, especially the first one. A gain slope of -6.0 dB per octave for the device was assumed and the input matching circuit was designed to compensate for this slope and to obtain an excellent match at 2.7 GHz. The result is a flat gain and a maximum gain in the desired bandwidth. From the device modeling and characterization data the predicted associated gain was G-1dB=13.0 dB and the gain flatness was 0.5 dB. The simulation also showed an input return loss of more than 12dB across the bandwidth for half the device. However the full device return loss will be higher since a balanced configuration was selected and the two device sides are symmetric.

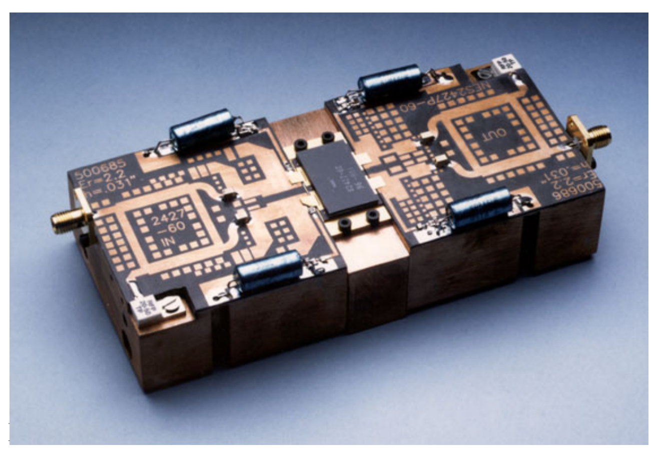
OUTPUT MATCHING CIRCUIT DESIGN

The design goal for the output matching network was to present the optimal load impedance for a two-tone signal at a defined output power with minimum loss. Since the NES2427P-60's device output optimal impedance for two-tone signal is not far from 50 ohm impedance, two sections of one-sixteenth wavelength Chebyshev impedance transformer circuit was selected. This circuit minimizes the dimensions and loss of the matching network. The impedance of the microstrip transmission lines were optimized to minimize the loss and maximize the return loss. The simulation showed that the loss of this output circuit was less than 0.2dB and the return loss was better than 19 dB across the bandwidth.

BALANCED AMPLIFIER

Figure 2 shows the complete balanced amplifier layout. The two-arm branch 90° hybrid which uses the same substrate as the matching circuit one, is integrated with the amplifier layout and does not require any additional connection. All the circuits are directly printed on the same Er=2.2, 31mil thick substrate. Standard 50 ohm loads are connected to the coupler isolated ports. The amplifier is compact and easy to assemble. The total dimensions of the amplifier are 13.2x6.0 cm^2.

Figure 2 Photo of NES2427P-60 Compact Balanced Amplifier



INPUT AND OUTPUT IMPEDANCE

The source and load impedances presented by the circuit to the device directly from simulation were measured versus frequency with a vector network analyzer. The experimental results showed that a good agreement between the measured and simulated impedances was achieved. Table 2 shows the comparison of the source and load impedance values simulated and measured. However a slight tuning was performed with the use of a vector network analyzer on the input and output matching circuits to obtain the exact simulated impedance values. Then the input, output and central blocks of the amplifier were assembled together and the device was mounted.

Table 2
Simulated and Measured Source and Load Impedances of Half NES2427P-60

Frequency (GHz)	Source Impedance of half NES2427P-60		Load Impedance of half NES2427P-60	
	Simulated	Measured	Simulated	Measured
2.4	6.2+j4.8	5.0+j7.4	20.2-j12.3	16.4-j8.7
2.5	7.1+j4.9	7.5+j7.1	19.5-j11.9	18.4-j8.9
2.6	7.4+j3.6	8.0+j4.0	18.8-j11.5	19.0-j10.6
2.7	4.9+j2.3	4.6+j2.8	18.2-j11.2	17.9-j12.4

RF PERFORMANCE

The amplifier was tested in with a 50 ohm system with a fixed broadband tuning corresponding to an optimum IMD3 performance CEL's High Power Automated Setup(7). The device was biased at Vds=10 V and Idsq=12 A. Figure 3 shows P-1dB & G-1dB performance versus frequency. The test results show a typical P-1dB of 48.5dBm and a typical G-1dB of 12dB. Figure 4 gives PAE and Ids versus frequency at 1 dB gain compression. It shows that the amplifier exhibits a typical PAE of 40% from 2.4 to 2.7GHz.

Figure 3
NES2427P-60 P-1dB & G-1dB vs Frequency

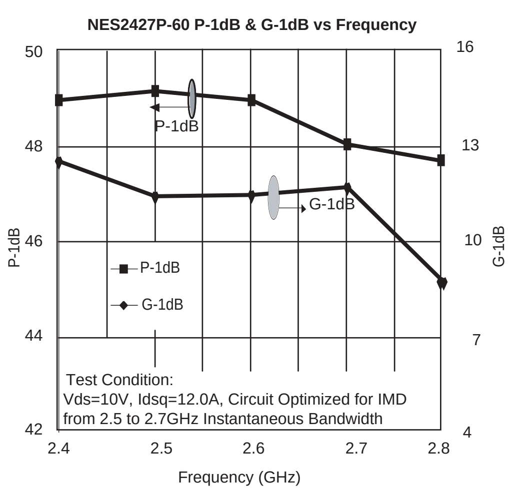


Figure 4
NES2427P-60 PAE & Ids vs Frequency

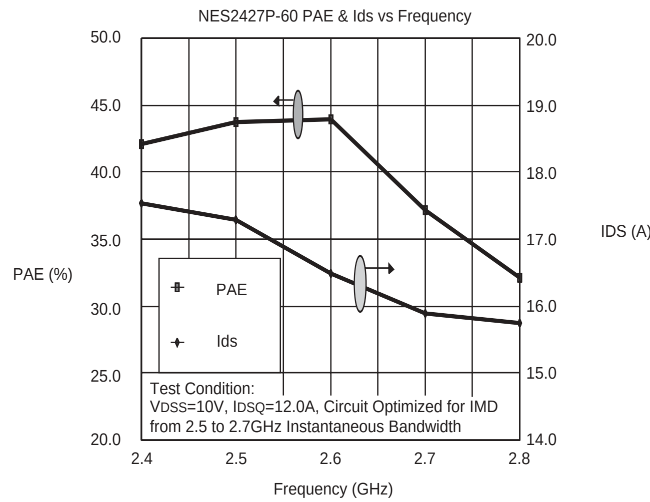
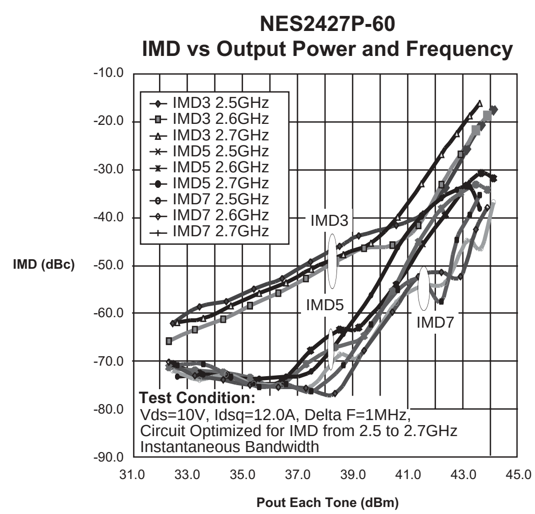


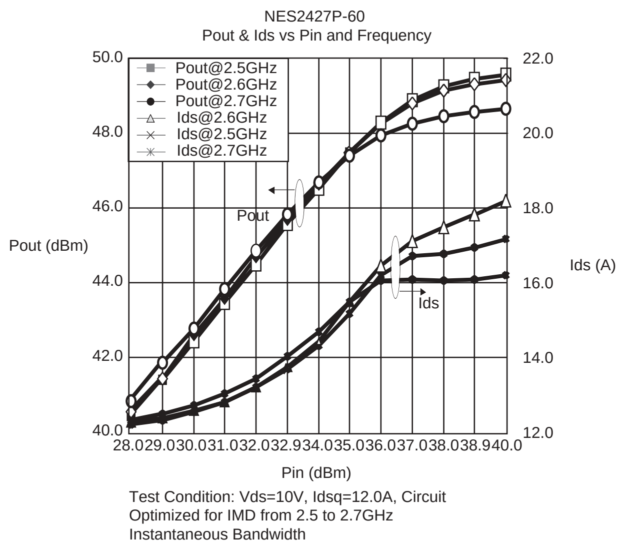
Figure 5 shows the IMD performance of this amplifier. These curves show that the amplifier has a good IMD performance with an IMD3 low than -42dBc at 40dBm output power each tone across the 2.5-2.7 GHz MMDS bandwidth.

Figure 5 NES2427P-60 IMD vs Output Power and Frequency



Pout & Ids versus Pin and frequency are shown in figure 6.

Figure 6 NES2427P-60 Pout & Ids vs Pin and Frequency



The amplifier input return loss in the 2.5-2.7 GHz bandwidth was better than 15.0 dB, which is better than the expected return loss for a push-pull configuration.

PERFORMANCE VERSUS CURRENT

The amplifier IMD performance was measured with a fixed tuning at constant, Vds=10 V, and at constant frequency, 2.7 GHz, versus Pin and Idsq. The figures 7, 8 and 9 show respectively IMD3, IMD5 and IMD7. The curves show, as expected, that this amplifier exhibits the best IMD3 performance at any Pout level when biased at the highest Idsq, 12 A. The maximum Idsq is limited only at Vds=10 V by the maximum recommended channel temperature which is 150℃.

Figure 7 NES2427P-60 IMD3 vs Idsq and Pout at 2.7GHz

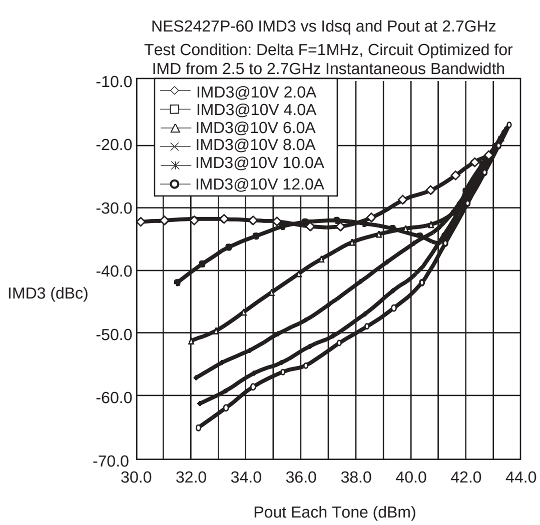


Figure 8 NES2427P-60 IMD5 vs Idsq and Pout at 2.7GHz

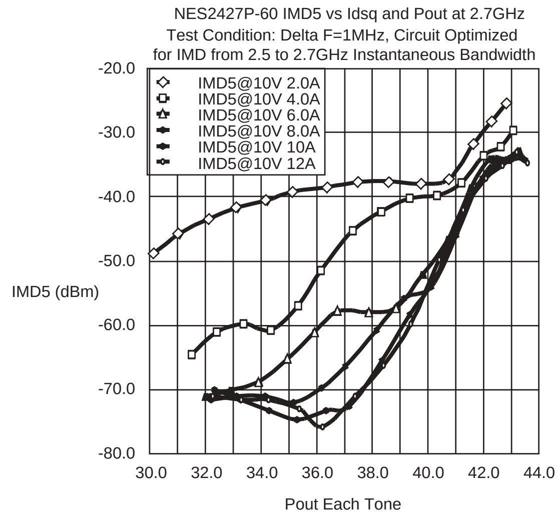
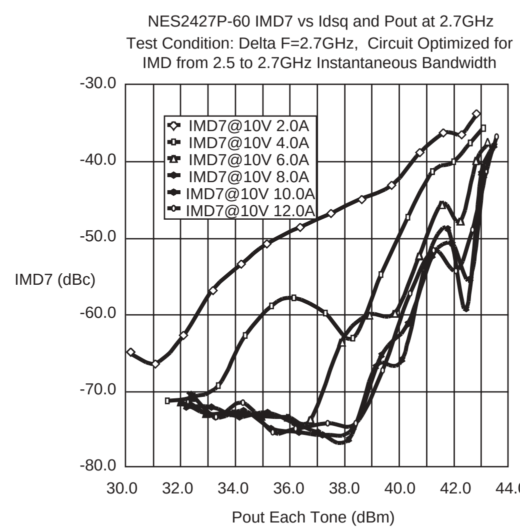


Figure 9 NES2427P-60 IMD7 vs Idsq and Pout at 2.7GHz



THERMAL CONSIDERATIONS, MAXIMUM IDSQ AND CLASS OF OPERATION

The MTTF of GaAs power devices is limited by their channel temperature. It is important for the amplifier designers to be able to calculate this temperature for their applications from the device power dissipated, the case temperature, and its thermal resistance (Rth). This calculation is not as simple as it may appear since the Rth of GaAs devices is a strong function of the device flange temperature and the channel temperature, or the power dissipated. The NES2427P-60 data sheet and CEL's application note(8) AN1032 give the information necessary to calculate Rth versus the flange and channel temperatures, or power dissipated.

The NES2427P-60 data sheet gives Rth=0.76 K/W maximum for Tf=25℃, Vds=10 V, Ids=12.0 A and recommends a maximum channel temperature of 150℃. This channel temperature corresponds to a MTTF of $2.4x10^6$ hours. From these data and with the help of the application note, the maximum Idsq can be calculated versus the device flange temperature.

As example for a maximum flange temperature of 52℃, the maximum power dissipated corresponding to a channel temperature of 150℃ is Pdiss.=120W. It means the maximum quiescent drain current (Idsq) for Vds=10 V and a flange temperature of 52℃ is 12.0 A.

This current is relatively high but it is lower than half of the device saturated drain current (Idss) which is 36 A typical. If the standard definition of class A for power devices is used, Idsq=12.0 A does not correspond to this device for a class A operation but to a class A-B one.

VII. CONCLUSION

A balanced compact high linearity power amplifier using a "Twin" device, NES2427P-60, was designed for the MMDS application. It was confirmed that all the targeted RF performance could be met successfully and a close agreement was obtained between simulated and actual performance. It delivers a power of 40 dBm each tone with an IMD3 between -43 and -46dBc and exhibits a P-1dB of 48.5dBm with a G-1dB of 12dB and a PAE of 40 %. The amplifier was fully characterized including IMD performance versus Idsq. The test results show that this compact balanced amplifier demonstrates a state-of-the-art performance in terms of linearity, Pout and efficiency across the 2.5-2.7 GHz bandwidth. This amplifier is very compact, uses an inexpensive substrate, and the splitter and combiner are printed and integrated to the amplifier layout without any additional connections. The choice of a balanced configuration results in a stable amplifier with an excellent external match without any compromise concerning the linearity.

REFERENCES

1. NES2427P-60 data sheet, visit CEL on the Web at http://www.cel.com

2. L. Max, "Balanced Transistors: A New Option For RF Design" Microwaves, June 1977.

3. L. Max, "Apply Wideband Techniques To Balanced Amplifiers" Microwaves, July 1980

4. G. Sarkissian, "A S-Band Push-Pull 60-Watt GaAs MESFET For MMDS Applications" 1997 IEEE MTT-S Digest

5. R. Basset, "Three Balun Designs For Push-Pull Amplifiers" Microwaves, July 1980

6. D. Raicu, "Design of Planar, Single-Layer Microwave Baluns" 1998 IEEE MTT-S International Microwave Symposium digest

7. R. Basset, "Automated Test Equipment For High Power Solid state Device Development And Characterization" 47th ARFTG Conference Digest, June 1996

8. Application note AN1032 "Microwave Power GaAs Device Thermal Resistance Basics", visit CEL on the Web at http://www.cel.com

California Eastern Laboratories

Exclusive Agents for NEC RF, Microwave and Optoelectronic semiconductor products in the U.S. and Canada

4590 Patrick Henry Drive, Santa Clara, CA 95054-1817
Telephone 408-988-3500 • FAX 408-988-0279 •Telex 34/6393
Internet: http:/WWW.CEL.COM