

# AN1036

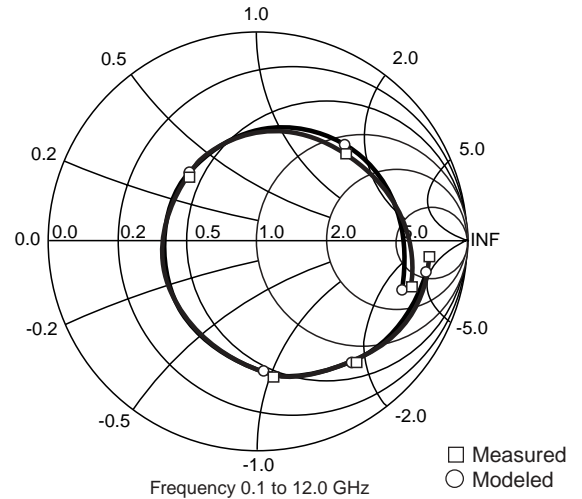
## Effects of Parasitics in Circuit Simulations

### Abstract

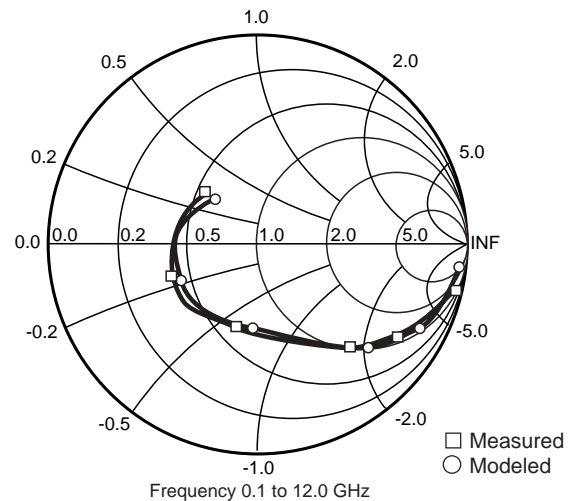
Including the proper parasitics in a nonlinear simulation can make the difference between an accurate prediction of circuit performance with minimal on-bench tuning and a design that requires significant modification after prototyping. This paper discusses the inclusion of parasitics in a low noise amplifier designed for the Bluetooth RF standard using the NE662M04, NEC's latest generation of silicon bipolar junction RF transistor. **California Eastern Laboratories** provides this circuit as an evaluation board to its customers. Circuit schematics and measured vs. simulated data with varying levels of circuit complexity graphically illustrate the effects of parasitics on the simulated results.

### NLM Verification

The first step in any nonlinear simulation is to confirm the validity of the nonlinear model at the bias and frequency range of interest. This should be performed to the manufacturer's measured s-parameter data. If the particular bias of interest is not available, confirm the model to the nearest available bias. **Figure 1** through **Figure 4** confirms the model is appropriate at the circuit design bias of 3V, 5mA and over a frequency range of 0.1 GHz to 12 GHz. The model also matches measured gain performance at 2V, 10mA and 2 GHz to better than 3% error and P1dB performance at the same bias to 7% error. Modeled Nfmin deviates from measured data by 4% error at a device bias of 2V, 5mA and the application frequency of 2.4 GHz. This information indicates the transistor is modeled correctly for this application and if the rest of the circuit is properly represented, the goal of minimum tuning of the prototype should be achieved.



**Figure 1. NE662M04 Measured vs. Modeled S11**



**Figure 2. NE662M04 Measured vs. Modeled S22**

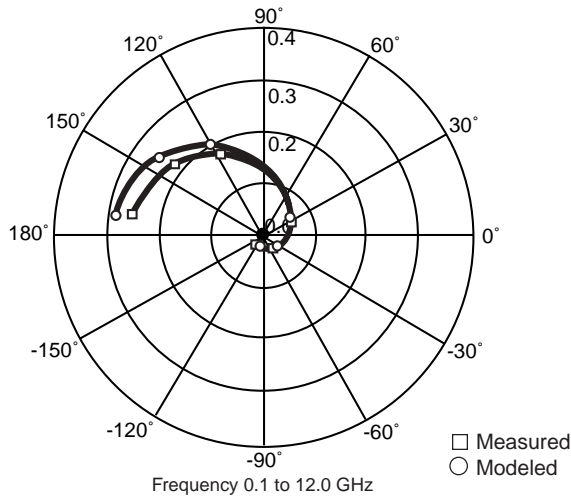


Figure 3. NE662M04 Measured vs. Modeled S21

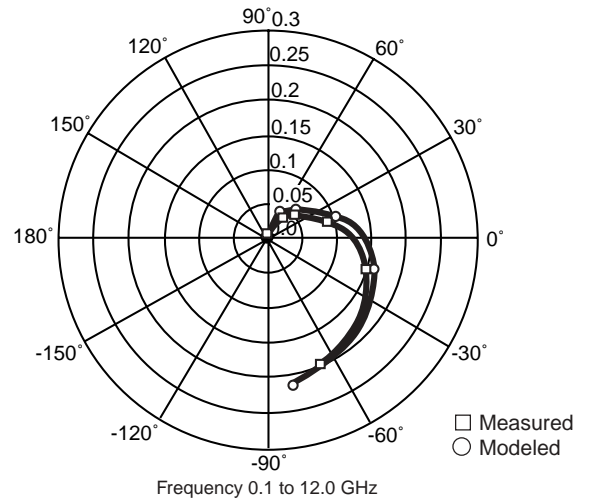


Figure 4. NE662M04 Measured vs. Modeled S12

Parameters	Specifications	Test Results	Simulation Results	Units
<b>LNA Section</b>				
Voltage	3	3	3	V
Current	5	5	5	mA
Operating Frequency	2400-2483.5	2400	2400	MHz
Gain	10	12	13.1	dB
NF	1.5	1.4	1.5	dB
1 dB Compression Point	-5.0	-0.5	-7.6	dBm
Input VSWR (50 Ohms)	2.5:1 (-9.5 dB)	-9.3	-11	dB
Output VSWR (50 Ohms)	1.5:1 (-14 dB)	-15.3	-16.5	dB

Table 1. Bluetooth Low Noise Amplifier: Specifications, Test Results and Simulation Results

### Simple Circuit Simulation

The design used to illustrate this example is a low noise amplifier optimized for the Bluetooth RF standard (Table 1) using the NE662M04. For information on the circuit design, please see reference [1]. California Eastern Laboratories provides with evaluation boards a description file, the circuit schematic, and a board layout. To demonstrate the effects of including parasitics in circuit simulations, the circuit schematic in Figure 5 as implemented in the HP-EEsof Series IV Libra simulator (Figure 6) was compared to data measured on the evaluation board. Transmission line lengths were measured on the evaluation board. Figure 7 through Figure 9 summarize the results of simulating the circuit without including board parasitics. It is readily apparent that the actual circuit is not being properly represented by the schematic of Figure 6.

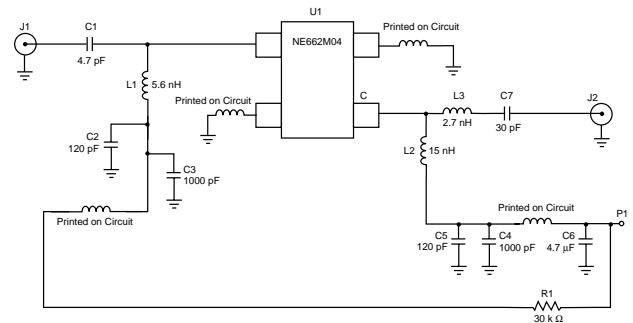


Figure 5. Evaluation Board Circuit Schematic

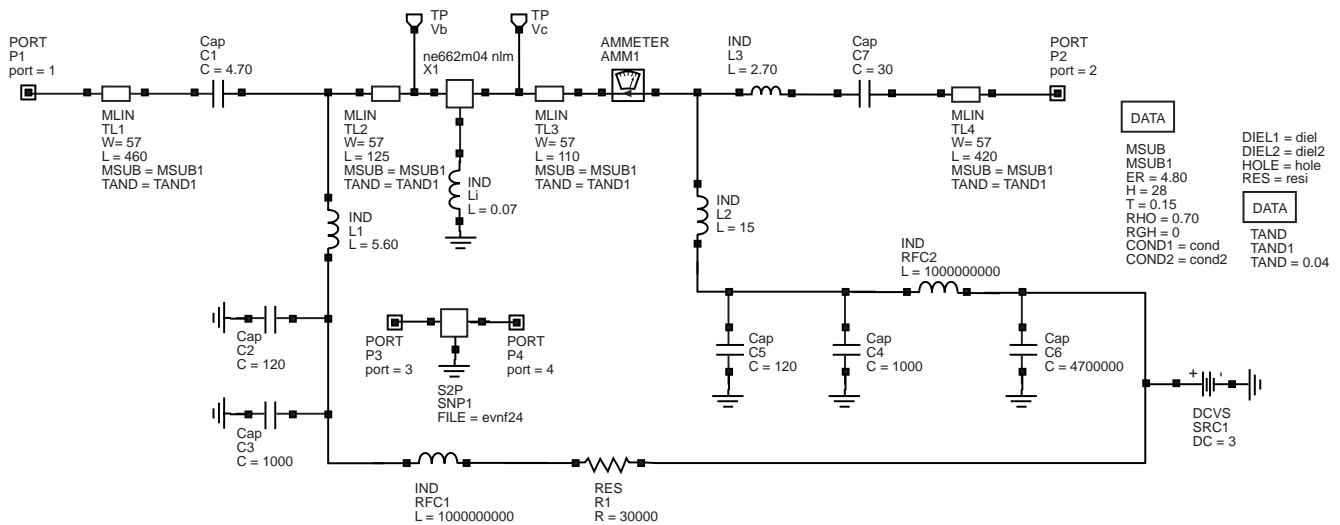


Figure 6. Simple Circuit Simulation Schematic

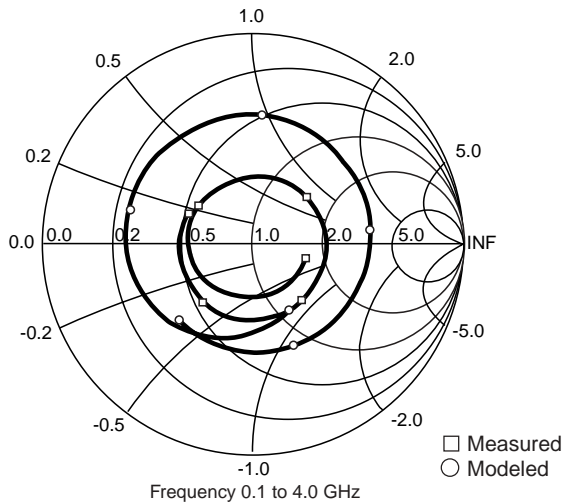


Figure 7. Simple Circuit - Simulation of S11

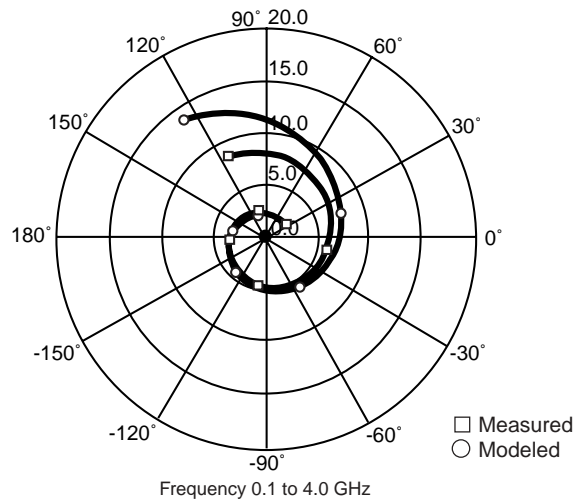


Figure 9. Simple Circuit - Simulation of S21

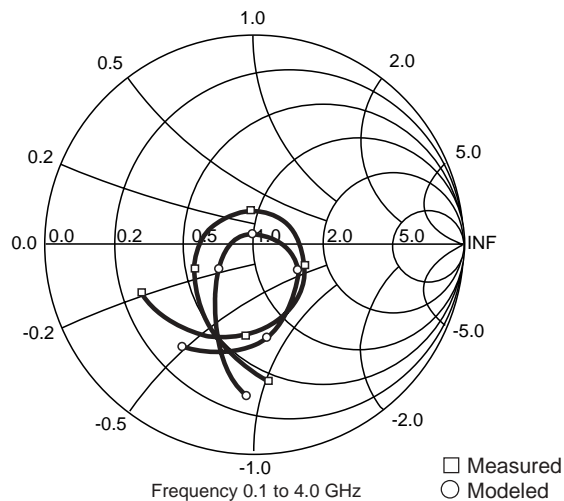


Figure 8. Simple Circuit - Simulation of S22

### Advanced Modeling

To improve the accuracy of the simulation, various techniques are used. One important parasitic to include is via holes. The via holes take into account the inductive loss through the substrate to ground. While these inductances are small, 40-60 pH/mm of substrate thickness [2], they can significantly alter simulation results when not included. As with all parasitic effects, the higher the operation frequency of the circuit, the greater the effect of the parasitics.

More accurate models of the actual transmission lines are used to account for the discontinuities at the junctions of different width microstrip lines. This discontinuity also occurs where discrete components are soldered to the

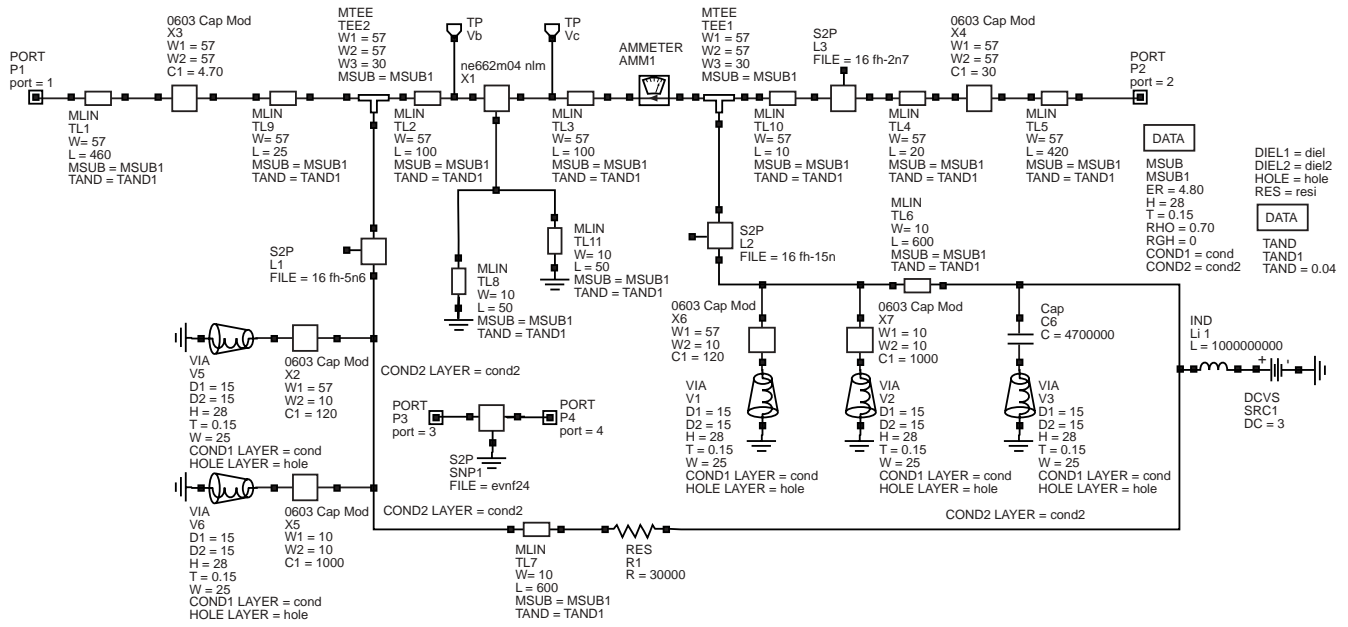


Figure 10. Final Simulation Schematic

board. Such junctions have scattering matrix representations which depend on the widths of the microstrip[3] and take into account the width-dependant inductances and capacitance of the junction. The long transmission lines (TL2 and TL3, Figure 6) on either side of the device are broken into two sections and a t-line is used where the shunt components are placed (TL9, TEE2, TL2, TL3, TEE1, and TL10 of Figure 10). The circuit in this example is fairly simple. For more involved circuits, more elaborate modelling of the transmission lines may be needed. The degree of complexity of all parasitic modelling will depend on the operation frequency of the circuit and how important it is to model the response of the circuit to higher order tones.

The third step is to model the discrete passive components with more accurate representations. The active device model has already been confirmed to be appropriate. There are several different choices to model the passives. Where available, actual measured s-parameters in the form of Touchstone formatted files (\*.s2p) can be used. Information available on the passive devices will vary according to manufacturer. If yield analysis needs to be simulated on the circuit, measured data is not a good option. Another choice is a model of the device which includes the parasitics present in the component package. Figure 11 and Figure 12 illustrate the models for the capacitor and the inductor used in the final simulation. A third option is to use the lossy lumped element models available in the simulator being used. Figure 13 is an example of a capacitor with Q as implemented in the Agilent-EESof Series IV Libra simulator[4]. In high-frequency applications where very accurate modelling of passive components is required, it is recommended that

passives be measured on the substrate that will be used and models developed from this characterization [5].

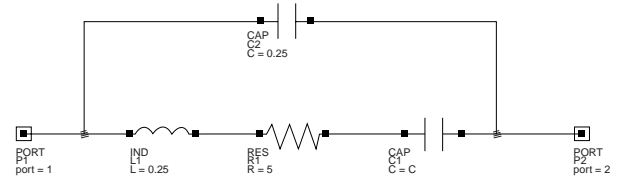


Figure 11. Capacitor Model Schematic

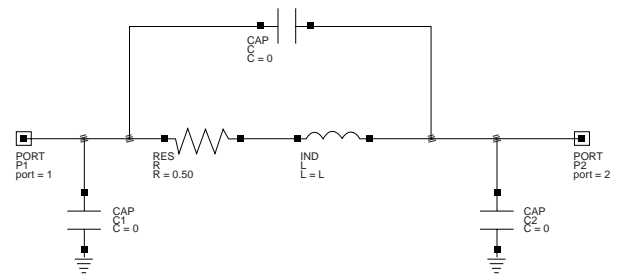


Figure 12. Inductor Model Schematic

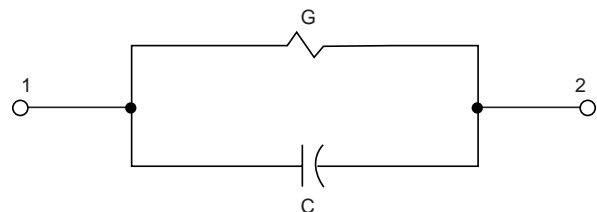
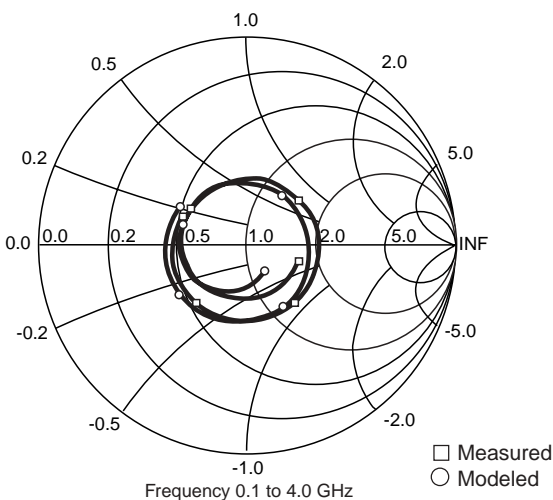
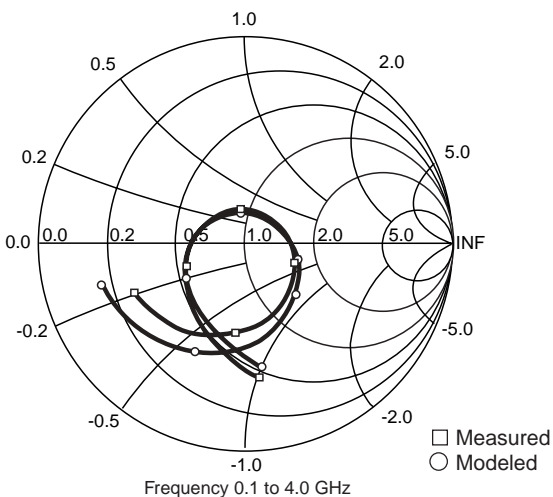


Figure 13. Simulator Capacitor Schematic

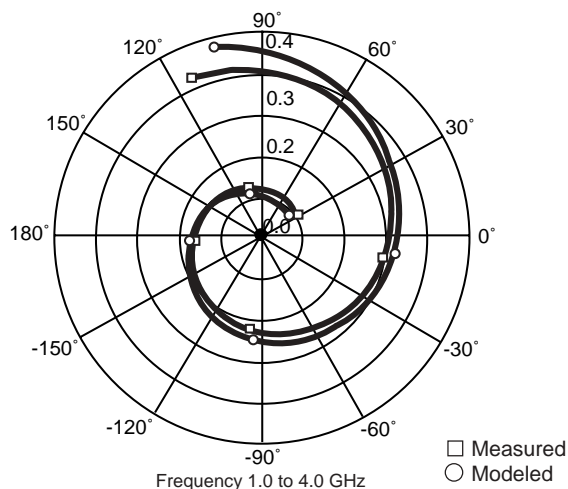
Some parasitics are not accounted for in this simulation. Elements not in the RF path, like the bias resistor R1 and the DC blocking capacitors are represented by ideal elements. The RF chokes, printed on the circuit board as meander lines, are represented by a straight transmission line. Simulating a more complex circuit does not improve the measured vs. modeled performance in this application. The final simulation circuit with added parasitics is shown in **Figure 10**. The much improved measured vs. simulated results are shown in **Figure 14** through **Figure 16**.



**Figure 14. Final Circuit - Simulation of S11**



**Figure 15. Final Circuit - Simulation of S22**



**Figure 16. Final Circuit - Simulation of S21**

## Conclusions

It has been shown that with careful modeling of all elements of a circuit, a design can be simulated which can be used to accurately predict circuit performance. This allows circuit designers to gain an edge in trimming the design cycle in both cost and time.

- [1] Bernard, Olivier, CEL Application Note # AN1037, "Optimizing a Silicon Bipolar LNA Performance for Blue Tooth Applications."
- [2] Pucel, Robert A., "Design Considerations for Monolithic Microwave Circuits," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-29, No. 6, June 1981, pp. 513-534.
- [3] Gupta, K.C., R. Garg, and R. Chadha, Computer-Aided Design of Microwave Circuits, 1981.
- [4] HP-EEsof Microwave & RF Circuit Design Circuit Element Catalog, pp. 9-20, 9-21.
- [5] Winslow, Thomas A. "Component Modeling for PCB Design," IEEE Microwave Magazine, Vol. 1, No. 1, March 2000, pp. 61-63.

## California Eastern Laboratories

Exclusive Agents for NEC RF, Microwave and Optoelectronic semiconductor products in the U.S. and Canada

4590 Patrick Henry Drive, Santa Clara, CA 95054-1817  
Telephone 408-988-3500 • FAX 408-988-0279 • Telex 34/6393  
Internet: <http://WWW.CEL.COM>

Information and data presented here is subject to change without notice. California Eastern Laboratories assumes no responsibility for the use of any circuits described herein and makes no representations or warranties, expressed or implied, that such circuits are free from patent infringement.