AN1034

APPLICATION NOTE

Designing VCOs and Buffers Using the UPA family of Dual Transistors

Abstract

This application note will review the process by which VCO (Voltage Controlled Oscillator) designers choose their oscillator's topology and devices based on performance requirement, real estate constraints and DC power consumption. Using a Personal Communication System (PCS) application as a practical example, this article will demonstrate a VCO and buffer design at 1.7 GHz using one of NEC's new UPA series space saving twin transistor packages. The required system specifications as well as the design's performance will be presented. The paper will then discuss Leeson's phase noise equation to gain insights into the design of low phase noise oscillators. Upon choosing an appropriate device and topology, a nonlinear simulation using HP-EEsof's SERIES IV will be performed to accurately predict the VCO performance. Measured results and practical "on the bench optimization" methods will be considered. Finally, as cost is of paramount importance to designers of commercial products, a total cost summary of the parts for the VCO and buffer module will be presented. While the design proposed may not yield the optimum design solution for all PCS applications, it does introduce a few important VCO design techniques that can be applied to other communication systems.

Design considerations

Designers of handheld wireless products share common goals: Higher performance, smaller size, lower DC consumption and lowest costs. To meets this goal, NEC developed the new UPA8XX Series Dual-chip silicon transistor array which provides two independently mounted devices within a single 1.25 x 2 mm six pin surface mount plastic package. With the different pin configurations, the UPA family can conveniently be used in a dual transistor or cascode operation. This family of devices can then be used for high-density designs where printed circuit board real estate is at a premium. One of such application for these dual transistor packages is a VCO and buffer design used as a component of cellular phone synthesizers.

PARAMETER	UNITS	SPECIFICATION	SIMULATION	MEASURED PERFORMANCE
Supply Voltage	(V)	3.35 V ± 0.25 V	3.3 V	3.35 V ± 0.25 V
Supply Current	(mA)	6.5 ± 2.5 mA	6.5 mA	7.25 mA
Control Voltage Range	(V)	0.7 to 2.7 V	N/A	0.7 to 2.7 V
Operating Frequency Range	(MHz)	1700 - 1730	1700 - 1730	1693 - 1738
Control Voltage Sensitivity	(MHz/V)	18 MHz/V min	Not simulated	20 MHz/V min
	(MHz/V)	22 MHz/V typ	Not simulated	22 MHz/V typ
	(MHz/V)	30 MHz/V max	Not simulated	N/A
Output Power (50 ohms)	(dBm)	-2.5 ± 2.5	-3	-1.5
Phase Noise at 300 Hz	(dBC/Hz)	-54	-60	-57.7
Phase Noise at 1 KHz	(dBC/Hz)	-66	-75	-72.8
Phase Noise at 10 KHz	(dBC/Hz)	-96	-97	-97.4
Phase Noise at 30 KHz	(dBC/Hz)	-106	-112	-107.3
Phase Noise at 60 KHz	(dBC/Hz)	-110	-120	-113.8
Phase Noise at 300 KHz	(dBC/Hz)	-126	-135	-128
Phase Noise at 900 KHz	(dBC/Hz)	-139	-150	-136.9
Freq. Pushing (V_{CC} = 3.35 V ± 0.25 V)	(KHz)	±800 max	N/A	±75
Freq. Pulling (VSWR = 2.0:1 at all phases)	(MHz)	±2	N/A	±1
Temperature Stability (-30° C to +80° C)	(MHz)	±6	Not simulated	±5.3
Harmonics	(dBC)	-10 min	-12	-10 min
Spurious	(dBC)	-80 min	Not simulated	-80 min
Output Impedance (in a 50 Ω system)	N/A	VSWR ≤ 2.0:1	VSWR ≤ 1.6:1	VSWR ≤ 1.2:1
Operating Temperature	(°C)	-30° C to +80° C	Not simulated	-30° C to +80° C

Table 1. PCS VCO: Goal, simulation and test results.

Specifications

In such a system application, the VCO must exhibit a low phase noise in order to meet the digital modulation scheme and Bit Error Rate requirements. It also has to meet the standard "below 3.5 V" DC voltage supplied by the batteries and needs the lowest DC supply draw to lengthen battery life. The buffer was a necessary addition to isolate the VCO from any output load variations and to provide the required output power. Meeting simultaneously the output power and load pull specification directly with a stand-alone oscillator would be exceedingly difficult and costly given the current draw constraint. Alternative would include circulator, isolators or passive attenuators. The phase noise specifications were as equally challenging given the limited tuning range of 0.7 to 2.7 volts and the varactor's influence on phase noise. Finally, portability drives the need for a design that is both compact and light. These last needs were met by using 0402 (40 mils by 20 mils) SMT technology components and by laying out the components in a tightly enclosed topology. These choices resulted in a .475" by 0.450" by 0.11" final design that also includes a grounded metal shield and the coaxial resonator. The enclosed **Table 1** summarizes the design goals, simulated performance and final laboratory results.

Device choice and characteristic

The UPA827TF contains two NE686 transistor dies chosen from adjacent position on the fabrication wafer. This particular transistor was chosen for its excellent microwave performance at low current and bias voltages up to 3 GHz. At a bias point of Vce = 2 volts and Ic = 2 mA, the NE686 demonstrates a gain bandwidth product of over 12 GHz, more than sufficient for an L-band oscillator. Under these conditions, it also provide a low 1/f Noise characteristic [2] and an excellent noise figure, both of which will yield superior phase noise performance. The package type chosen for this oscillator and buffer was the UPA827TF because it is extremely compact and ideal for applications requiring two transistors where board real estate is scarce commodity.

Oscillator Phase Noise Theory

As mentioned above, one of the most challenging aspects of VCO design is meeting the phase noise specifications. Studying Leeson's equation [1] in respect to oscillator phase noise provides some insight into the factors that affect the noise performance of a VCO:

$$L(fm) = 10\log\left[\left(1+\frac{f_0^2}{(2f_mQ_1)^2}\right)\left(1+\frac{f_c}{f_m}\right)\left(\frac{FkT}{2P_S}\right)+\frac{2kTRK_0^2}{f_m^2}\right]$$

Leeson's Equation **(1)**

Where L(f_m) is the ratio of the sideband power in a 1 Hz bandwidth at an offset of f_m to the total output power generated by the oscillator in dBC/Hz.

- f_0 = Carrier center frequency.
- f_m = Frequency offset from the carrier center frequency.
- f_c = Flicker corner frequency of the semiconductor device used as the oscillator.
- Q_P = Loaded Q of the tuned circuit (resonator).
- F = noise factor of the active device (not to be confused with the noise figure).
- kT = Boltzman constant time room temperature (=4.1 * 10^{-21} at 300K (room temperature)).
- P_S = Average power at oscillator input.
- R = Equivalent noise resistance of tuning diode.
- K_0 = Oscillator voltage gain in volts/Hz.

Leeson's equation provides some powerful insights into which parameters will yield the best phase noise performance in a VCO [3]. In order to lower the phase noise, a number of rules should be respected:

Rule 1. Maximize the loaded Q of the tuned circuit in the oscillator.

In most designs, there usually is a trade-off between the Q-factor of the oscillator, its size and its price. A dielectric resonator is considerably more expensive than an LC tank or a tuned wire. However, the low Q-Factor of an LC tank and the variation in high volume manufacturing of a tuned wire would not allow the design to consistently meet the phase noise specifications without individual readjustment of the oscillators. Consequently, the design will incorporate a quarter wavelength coaxial resonator. In this case, a larger resonator will have a higher Q. However, since size is also critical in our design (a handheld application) we will compromise with the smallest coaxial resonator available. We will use a 2 mm shorted quarter wavelength coaxial resonator with a typical unloaded Q of 215. The resonator can also be obtained in 1 % tolerances, which will improve repeatability in a high volume manufacturing environment.

Rule 2. Choose an active device that has a low flicker corner frequency.

A bipolar transistor biased at a low collector current will keep the flicker corner frequency to a minimum, typically around 6 to 15 KHz (Most semi-conductor manufacturers can provide the f_c of their devices as well as the 1/f characteristic [2]). As explained earlier, the NE686 transistor is ideally suited for this low current and low voltage microwave applications because of its high gain bandwidth product and low noise performance.

Rule 3. Maximize the power at the input of the oscillator.

This represents one of the trade-offs in our design that makes achieving the phase noise specifications a bit more challenging. In order to increase the power at the input of the oscillator, the current has to be increased. However, a low current consumption is critical to preserving battery life and keeping a low f_c. In a practical application, the designer will set its current based on output power required to drive the system (typically a mixer) and meet battery life requirements, meeting phase noise is then secondary and will need to be achieved through other means.

Rule 4. Choose a varactor diode with a low equivalent noise resistance.

This again, is a tricky part in the design because the varactor diode manufacturers do not measure or specify this parameter. The best approach is then empirical; by obtaining varactors from several vendors and experimentally finding out which one yields the lowest phase noise in the VCO circuit and thus has the lowest equivalent noise resistance.

Rule 5. Keep the voltage tuning gain (K_0) to the minimum value required.

This usually is the most challenging compromise faced by VCO designers. The VCO must meet a 22 MHz/V voltage tuning sensitivity for K_0 . Yet, we also need to keep the phase noise to a minimum. The thermal noise from the equivalent noise resistance of the varactor works together with the tuning gain of the VCO to generate phase noise. In fact, it will be shown in the testing phase that this compromise will be the limiting factor determining our phase noise performance.

Choice of topology

Figure 1 shows the topology that will be used for this VCO design. The circuit will use the NE686 devices contained within the UPA827TF miniature (1.25 mm x 0.6 mm) TS06 package for a different application. $U_{1:1}$ used as a Colpitt oscillator, is the transistor designed in a common collector configuration and which utilizes the feedback voltage divider C_1-C_5 to unstabilize the device. Therefore, the impedance that will be seen by the resonator on $U_{1:1}$'s base will be negative and the system is classified as a reflective oscillator. The system's thermal noise will create a signal build-up between the Bipolar and the resonating tank that will build to an oscillation at a frequency guided by the resonator. The coaxial resonator T_1 is lightly coupled to the transistor's base through C_2 while the Varactor diode D_1 is coupled into the resonator circuit via C_3.
$U_{1:2}$ is the buffer transistor designed in a classical common emitter configuration. C_7 is the coupling capacitor that taps some of the energy out of the VCO. The smaller the amount of energy drained out of oscillating circuit, the better the loaded Q factor and therefore the better the phase noise performance. However, the drawback is a low output power from the complete circuit. No attempt was made to match the buffer input to the VCO output impedance. L3 and C8 match the output of the buffer to 50 ohms.

When choosing the resonator, a good rule of thumb that works well with this VCO topology is to choose a component that is 15 to 20 % above the VCO operating frequency. A resonator of 1950 MHz self-resonating frequency is chosen for the computer simulation. The coaxial resonator is a coax structure constructed of ceramic material with a dielectric constant of 39. The ceramic is coated with silver and is shorted to ground on one end, to form a quarter wavelength resonating structure at a given frequency. Application notes on coaxial resonators can be obtained from reference [4]. **Figure 2** shows the dimensions of the resonator.
Concerning the feedback capacitors in the Colpitt, the ratio of C_1 to C_5 is more important than the capacitor's actual values. A good place to start is with a one to one ratio. The loaded Q of the resonator circuit can be augmented by increasing C_5 or reducing C_2. Doing so however, reduces the loop gain in the oscillator, and enough loop gain must be maintained to guarantee oscillation start-up under all conditions (mainly under different temperatures and system output loads). The value of R_1 also affects the oscillator loop gain. As in a common collector amplifier, the lower the impedance in the collector circuit the more loop gain the circuit will have. This resistor provides the designer another means of controlling the loop gain of the oscillator since a good oscillator design has just enough loop gain to guarantee reliable oscillation start-up. If there is to much loop gain the oscillator will operate in deep compression which will load the Q of the resonator circuit because the input impedance at the base of the transistor is very low when current saturation occurs. The resistor also tends to subdue the level of the harmonics. L_1 is chosen as an RF choke to provide a high impedance in the emitter circuit and ensure that most of the oscillator power is fed back to the base of $U_{1:1}$ instead of being dissipated in R_3. R_3 is used for current feedback thus providing a stable DC bias point that will be independent of the beta of the transistor.
C_2 defines the amount of coupling between the active device and the resonator. The lighter the coupling (a smaller value of C_2), the better the loaded Q of the resonator is, which results in a better phases noise performance. However, the compromise is a reduced output power and the potential for the VCO not to start under all operating conditions (especially at higher temperatures when current gain is reduced). Designing the system with too light of a coupling may also results in a sensitive design which may yield potential manufacturing problems.
The final tuning component of the oscillator, C_3 sets the voltage tuning gain of the oscillator. This capacitor should keep the coupling as light as possible while maintaining the required frequency tuning range of the VCO so that the varactor's phase noise contribution is reduced to a minimum. L_2 is chosen as an RF choke. C_4, C_6, and C_9 are chosen as RF bypass capacitors.

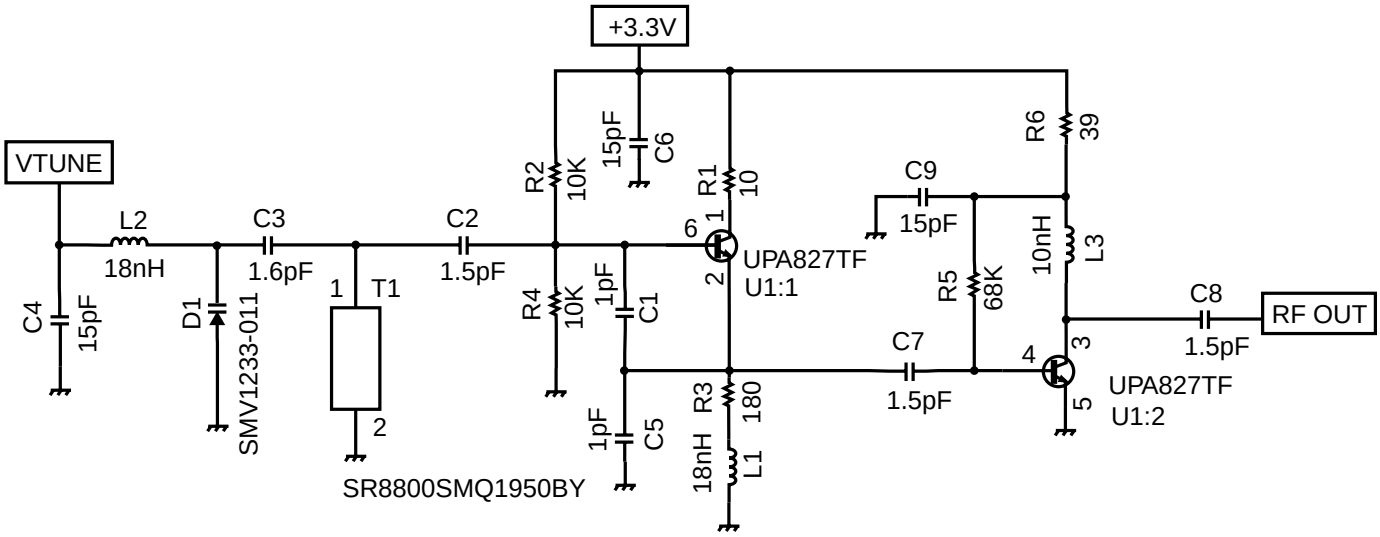

Figure 1. VCO Schematics.

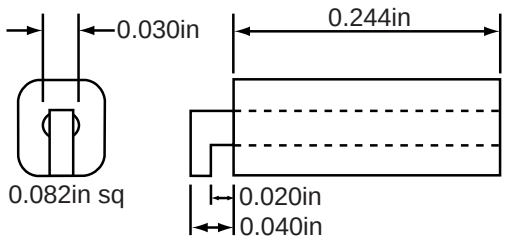

Figure 2. 1.95 GHz Coaxial Resonator dimensions.

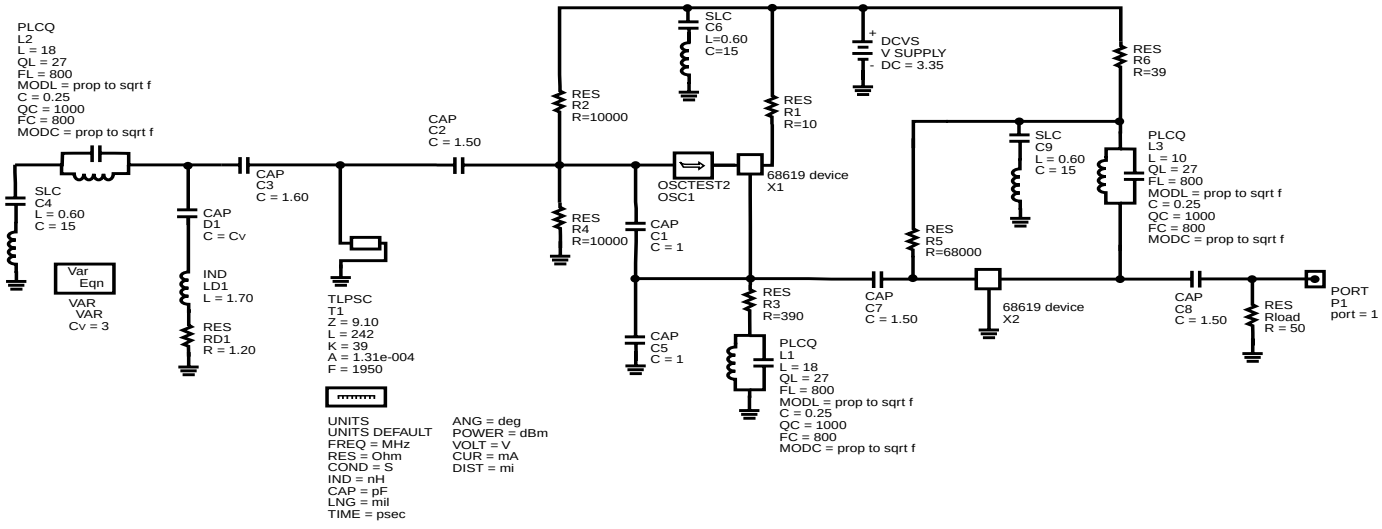

Figure 3. Nonlinear Circuit Simulation Schematic.

Circuit Simulation

The nonlinear model for the NE68619 was used for the simulation as a close approximation to the UPA827TF and is shown in **Figure 4.** The package parasitics will be slightly different between the two devices, but at 1.7 GHz, this will not be critical and we can still count on a reasonably accurate simulation. Please note that the blocks X_1 and X_2 in the simulation schematic of **Figure 3** represent the circuit shown in **Figure 4.**

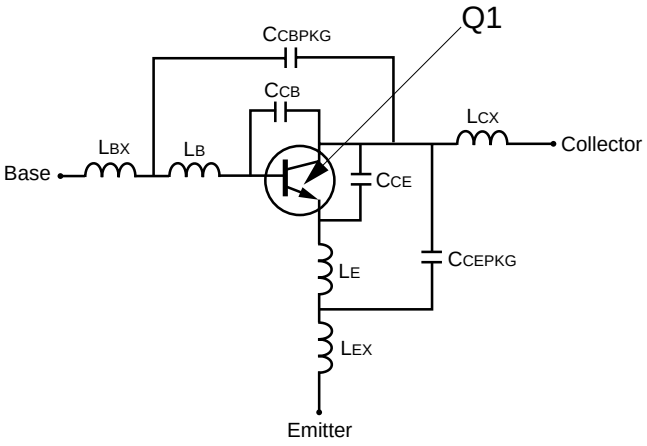

Figure 4. Nonlinear Model for the NE68619.[1]

The simulation parameters for the resonator are provided by a computer program called COAX (distributed free of charge) from Transtech Inc. [3]. COAX lists the parameters used by HP-EEsof's Series IV program for a physical transmission line. **Table 2** shows the parameters for HP-EEsof's Series IV simulator.

LIBRA parameters for TLINP element
Z = 9.1 (characteristic impedance)
L = 0.242 (length in inches)
K = 39 (effective dielectric constant)
A = 0.131 (loss in dB per inch)

Table 2.

Note that particular attention was taken to account for many of the component parasitics in the simulation to increase the accuracy of the simulation and reduce the amount of board tuning during the laboratory circuit testing.
The varactor chosen for this design is the SMV1233-011 from Alpha Inc. This varactor (C_v) is modeled as a capacitor in series with a resistor and an inductor. The varactor capacitance is assigned the variable C_v. C_v is swept from 1.8 to 3.8 pF to simulate a tune voltage that varies from 0.7 to 2.7 volts. The linearity of the tuning is as this point of no concerns since the intent is to verify that varying the varactor's capacitance does provide a monotonous tuning of the VCO frequency while keeping the output power to some extent constant.

The VCO's output matching network (L_3 and C_8) was first optimized for the best output return loss in a linear test bench. **Figure 5** shows that the predicted output VSWR is less than 1.62 over the band of interest.

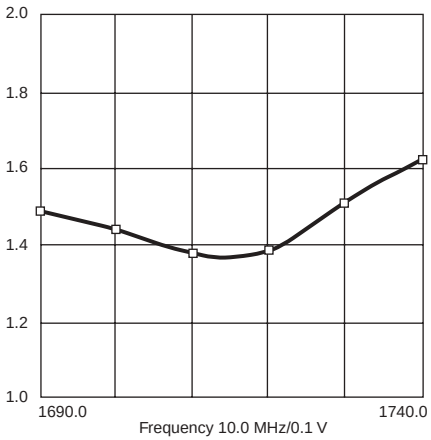

FIGURE 5. Output Matching of the VCO Buffer Amplifier

Libra's oscillator test bench was then used to predict the VCO's nonlinear performance. **Figure 6** shows the test bench setup.

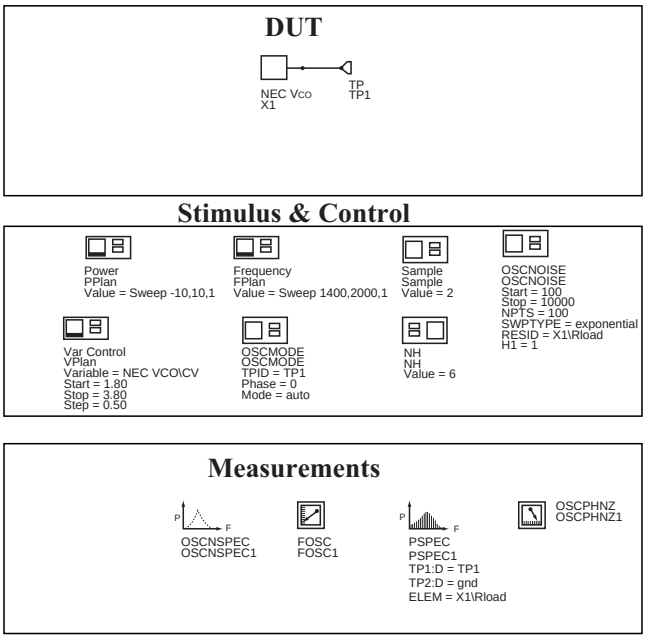

Figure 6.

Libra uses the **"Osctest"** element (see **Figure 3**) to inject a swept AC noise signal into the oscillator loop (to get a start-up condition) and uses an iterative process to find the oscillator steady state frequency and power. The components in Libra were tuned until a frequency range of 1698 to 1745 MHz was predicted when C_v was varied from 3.8 to 1.8 pF. C_v was then set to 2.8 pF and the VCO was simulated to predict its

Note 1: Refer to the NE68619 datasheet for full documentation of the nonlinear model.

output spectrum and phase noise. **Figure 7** shows the predicted output spectrum. As can be seen on the graph, a fundamental power of -3 dBm with harmonics of at least -12 dBC are predicted. **Figure 8** shows that the predicted phase noise at a 10 KHz offset is -97 dBC/Hz.

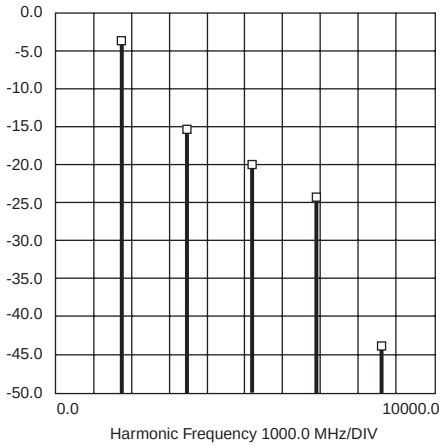

Figure 7. Output Spectrum of the VCO.

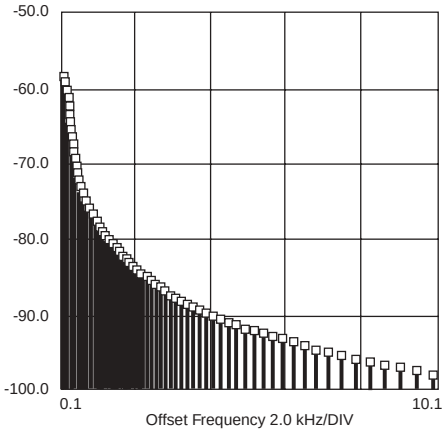

Figure 8. Simulated Phase Noise of the VCO.

The VCO printed circuit board was then laid out. The package size for the inductors, capacitors, and resistors chosen were 0402 because of real estate considerations. The total space enclosure achieved by the VCO and buffer circuit is 0.450 by 0.475 inches, including the grounding outline for a shield over the entire circuit. **Figure 9** shows the PCB artwork for the complete module. For testing convenience, a larger evaluation printed circuit board was constructed to accommodate an SMA connector, DC power, ground, and tuning connections. **Figure 10** shows a photograph of the evaluation board. The dime placed next to the VCO circuit provides the reader with a feel for how compact the design is. The coaxial resonator has a height profile of 0.080 inches. When 0.030 inches of extra height is allowed for a shield over the circuit the total height of this VCO and buffer assembly is kept to 0.110 inches.

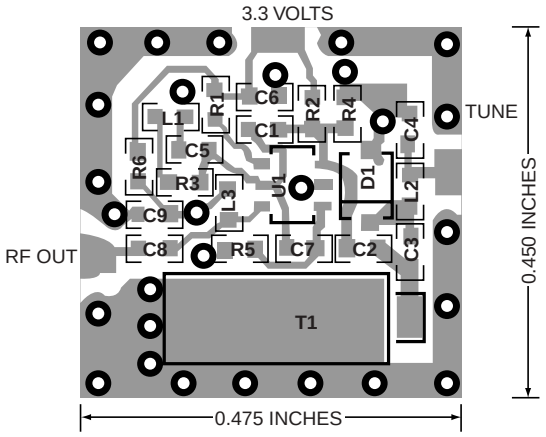

Figure 9. Art Layout of the VCO/Buffer.

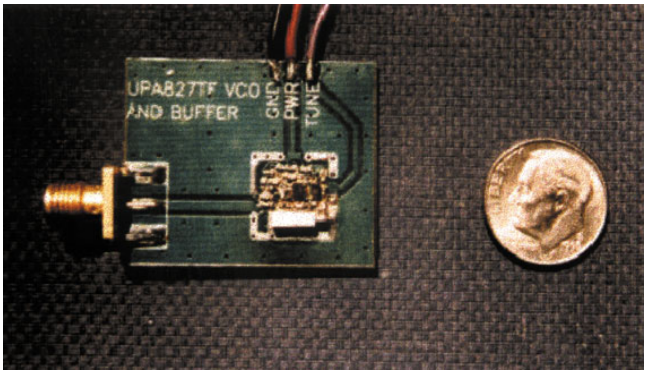

Figure 10. The Prototype Board Assembled and Tested for this Application Note.

Circuit Testing

Upon achieving satisfying results with the simulation and choosing the appropriate circuit values for the different components, a prototype board was constructed and tested for compliance with the proposed specifications. The VCO tuned from 1521 MHz to 1580 MHz when the varactor voltage was varied from 0.7 to 2.7 volts. The phase noise at a 10 KHz offset was -89 dBC/Hz. The output power was -2 dBm. The second harmonic was -10 dBC. The buffer's output return loss was measured to be -7.5 dB. The total current consumption of the VCO and buffer was 7.3 mA. Although the nonlinear computer simulation did not perfectly predict the VCO behavior, it provided a good starting point to pursue "on the bench" optimization.

To improve the output return loss, L3 was changed to 6.8 nH. This tuning resulted in achieving an output VSWR of less than 1.2:1 over 1700 to 1730 MHz. This change also increased the output power to 0 dBm. To improve phase noise and reduce the tuning gain of the VCO to the desired 22 MHz per volt, the value of C3 was reduced to 1.2 pF. To increase the loaded Q of the resonator circuit, the coupling capacitor C_2 was also reduced to 0.5 pF. Again, caution must be exercised

when reducing the coupling to the resonator. If the coupling is too light, the oscillator may not start under certain conditions. The worst case condition for this oscillator topology is when V_{Tune} is set at zero volts. A good way to check if C_2 is large enough for reliable oscillator start up is to monitor the output power of the VCO with zero volts on the tune line. The power with V_{Tune} at zero volts should be within 1 dB of the power with V_{Tune} at 2.7 volts. If C_2 is too small, the output power of the VCO will fall off sharply when V_{Tune} approaches zero volts or the oscillator may stop completely. One good reason to use a transistor with a high Ft such as the NE686 is that C_2 can be small and oscillation start-up will be reliable simultaneously. With such a light coupling, the coaxial resonator had to be changed to a 2000 MHz resonator to get the frequency up to 1700 MHz. Upon completion of all this fine tuning, the phase noise had improved to -97.4 dBC/Hz at a 10 KHz offset.

In order to ensure that the loaded Q of the resonator circuit is not the limiting factor in phase noise performance, the varactor can be replaced it with a fixed capacitor. The capacitor value should be in the mid-tuning range capacitance of the varactor. This makes the circuit a free running oscillator and the phase noise performance can be measured without the effects of the varactor equivalent noise resistor. While replacing the varactor D_1 with a 2.7 pF capacitor, the phase noise was measured to be -102 dBC/Hz at a 10 KHz offset frequency. Thus, the equivalent noise resistance of the varactor accounts for a 4.7 dB degradation in the phase noise of the VCO. A VCO with a wider tuning range will see more of degradation due to the varactor. The varactor can reduce the Q of the resonator circuit but this effect is secondary to the varactor modulation due to its own equivalent noise resistance. One way of reducing this effect is to parallel two or more varactors of smaller value while keeping the same tuning curve [4]. This effectively reduces the equivalent noise resistance. The trade off here is cost and more real estate. **Figure 11.** shows the final circuit.

With the varactor D_1 back in the circuit, all of the VCO specifications were measured and a re reported in **Table 1.** As can be seen the measured specifications were either met or exceeded by this VCO design.

Table 4. shows the parts list for the VCO and buffer assembly. The total approximate cost for the entire circuit is $2.17 in 100K quantities.

Summary

This application note has demonstrated a VCO and buffer design at 1.7 GHz using one of NEC's new NPN space-saving dual transistor packages. The required performance specifications were presented. Leeson's phase noise equation was then discussed to develop some rules of thumb for low noise VCO design. HP-EEsof's Series IV was then used to predict and optimize the VCO performance. Measured results and practical "on the bench optimization" was then pursued. The result was a VCO that met all the specification goals for a typical PCS application. The techniques presented in this applications note can be used to design a VCO that is customized to the reader's requirements. The UPA827TF is an excellent choice for VCO and buffer design because of good microwave performance at low power biasing, compact packaging, and low cost. A very compact VCO and buffer design was presented that would cost just over $2.00 in 100K quantities for parts in production.

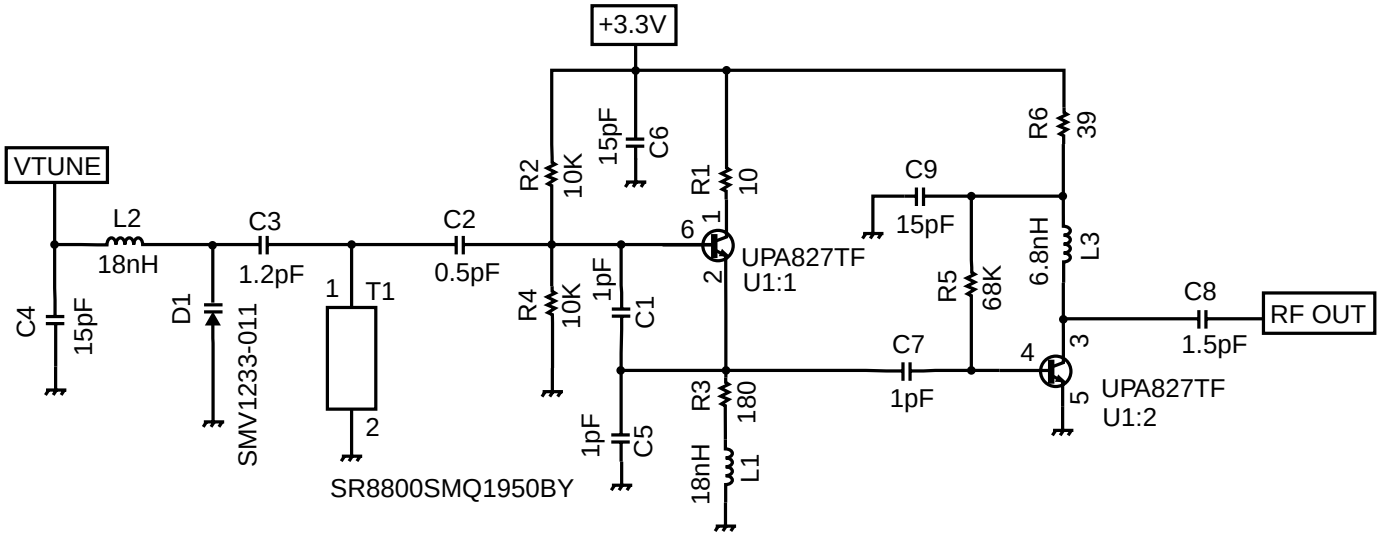

Figure 11. Final Optimized Circuit Schematics.

REFERENCE DESIGNATOR	DESCRIPTION	APPROXIMATE COST (100K QUANTITIES)
U1	UPA827TF, NPN dual microwave transistor (NEC)	0.40
T2	SR8800SMQ2000BY, 2000 MHz coaxial resonator (Trans Tech)	0.70
C1, C5, C7	1.0 pF NPO chip capacitor, 0402 package	0.015
C2	0.5 pF NPO chip capacitor, 0402 package	0.02
C3	1.2 pF NPO chip capacitor, 0402 package	0.015
C4, C6, C9	15 pF NPO chip capacitor, 0402 package	0.015
C8	1.5 pF NPO chip capacitor, 0402 package	0.015
L1, L2	18 nH chip inductor, 0402 package	0.15
L3	6.8 nH chip inductor, 0402 package	0.15
R1	10 ohm chip resistor, 0402 package	0.005
R2, R4	10K ohm chip resistor, 0402 package	0.005
R3	180 ohm chip resistor, 0402 package	0.005
R5	68K ohm chip resistor, 0402 package	0.005
R6	39 ohm chip resistor, 0402 package	0.005
PCB1	0.031 thick double sided FR4 printed circuit board	0.25
SHIELD1	Metal shield	0.20
	Total parts cost (approximate)	2.17

Table 4. VCO Billing of Materials.

References

[1] D. B. Leeson, **"A Simple Model of Feedback Oscillator Noise Spectrum,"** Proc. IEEE, vol. 54 p. 329, Feb. 1966.

[2] California Eastern Laboratories, **"1/f Noise characteristics influencing Phase Noise,"** AN1026.

[2] Dr. Ulrich L. Rohde, **"Designing Low-Phase-Noise Oscillators,"** QEX, October 1994,
p. 3 and 9

[3] Roger Muat, **"Designing Oscillators for Spectral Purity,"** Microwaves & RF, p. 140, July 1984.

[4] **COAX**, version 4.2, Transtech Inc.
To contact Transtech for a free copy of COAX call (301) 695-7065

[5] Randall W. Rhea, **"Oscillator Design and Computer Simulation,"** Noble Publishing, Atlanta, 1995.

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