CEL California Eastern Laboratories

AN1033

APPLICATION NOTE

NonLinear HJ-FET Model Verification in a PCS Amplifier

PCS Amplifier Design Part 3

I. Introduction

Lower development costs and shorter times to market of telecommunication subsystems require effective and accurate circuit simulation. This translates into designs that work at turn-on or with limited tuning. Simulation is now considered part of the standard design procedure. To perform extensive nonlinear simulations on a circuit, nonlinear models for the active devices need to be developed. This paper describes the steps involved in verifying a commercially available nonlinear Hetero-Junction Field Effect Transistor (HJ-FET) model. The non-linear model is then validated when it is used to predict circuit performance in a low noise PCS amplifier. The modeled results are then compared to measured data.

II. Model types

There are several types of models which can be developed to predict the behavior of an active device. One type of model is a linear model. A linear model is fairly easy to generate, easy to use, and is usually developed at a particular bias. The designer can relate parameter values to the equivalent circuit model, and a linear model can be used by both linear and nonlinear simulators. However, the linear model cannot be used to predict nonlinear performance such as compressed output power, mixing products, or intermodulation performance.

The nonlinear model consists of a series of analytical mathematical relationships where parameters have been linked to physical device behavior. Nonlinear models are more complex, but when properly developed can be used over a range of biases and can predict nonlinear behaviors. Nonlinear models are used to simulate mixer and oscillator applications and provide useful information on the linearity and output power of an amplifier.

III. Requirements for a nonlinear device model

Most amplifier designs, and other telecommunication subsystems such as mixers and oscillators, start with linear simulations. This first step usually requires only linear components such as measured S-parameters and noise parameters. With experience, the engineer can develop a feel for the practical problems involved in linear matching. Additionally, there are many well outlined references and design approaches to small signal simulations that yield accurate laboratory results on a first prototype.

However, for the nonlinear performance of such designs, the results are often less accurate and test bench tuning can result in considerable frustration. Developing a good understanding of nonlinear models, their expected performance and technical limitations can improve the accuracy of a circuit and reduce turn around time for a new design. The engineer can use the nonlinear model to optimize and center a design on such nonlinear device performance such as the output power of an oscillator, conversion gain of a mixer, or IP3 of a low noise amplifier.

IV. Choosing the nonlinear model

Once it has been established that a nonlinear model of a device would be useful, and supporting laboratory measurements have been taken, a nonlinear model must be chosen. The choice of model is determined by evaluating the DC characteristics of the device and comparing these measured characteristics to characteristics of available nonlinear models. Different models implement the DC I-V curve equations differently [1]. For the device under consideration, NEC's NE34018, it was determined Triquint's Own Model (TOM) would best represent the I-V curves because the HJ-FET showed an almost linear increase in drain current with increasing drain voltage at lower gate voltages and an approximately constant drain current with respect to increasing drain voltage at higher gate voltages (see Fig. 2).

V. Extracting the device model

Just as there is more than one nonlinear model to choose from, there is more than one method available for extracting model parameters. Parameter extraction methods range from expensive extraction software products to a more simple but less efficient method of optimizing model parameters until the model reflects the measured data within the range of interest. Whatever method is chosen, it is important to have an idea of how the model parameters affect the predicted results and what the appropriate limits are for the parameters. CEL currently has a process for developing an HJFET model. This is accomplished by extracting DC model parameters which reflect the measured I-V curves, and then the AC parameters are adjusted. Once the DC and AC performance of the model is satisfactory, the model can be optimized to fit measured power and noise data.

Model parameters affect more than one type of simulation response. For example, the model parameter Rg effects both the I-V curves and the S-parameters, and Cds effects both the S-parameters and output power. These dependencies are evaluated during the model extraction phase. The value of a parameter that results in the model providing the best S-parameter fit may not provide the best fit to measured power data. There is usually a trade-off when developing a device model over a wide range of biases and frequencies.

VI. Device model extraction results

The device model for the NE34018 was extracted over the following ranges:

DC: Vds=0V to 5V, Vgs=0V to -0.7V
AC: Vds=1V to 3V, Id=5mA to 40mA,
Frequency=0.5 GHz to 6 GHz

Power and IM3: Vds=3V, Id=20mA,
Frequency=2 GHz.

Fig. 1 and Table 1 present the final device model and Fig. 2-8 compare the results of the extracted device model to the measured data. S-parameter comparisons (Fig. 3-6) are shown at the desired PCS amplifier bias of Vds=3V, Ids=20mA.

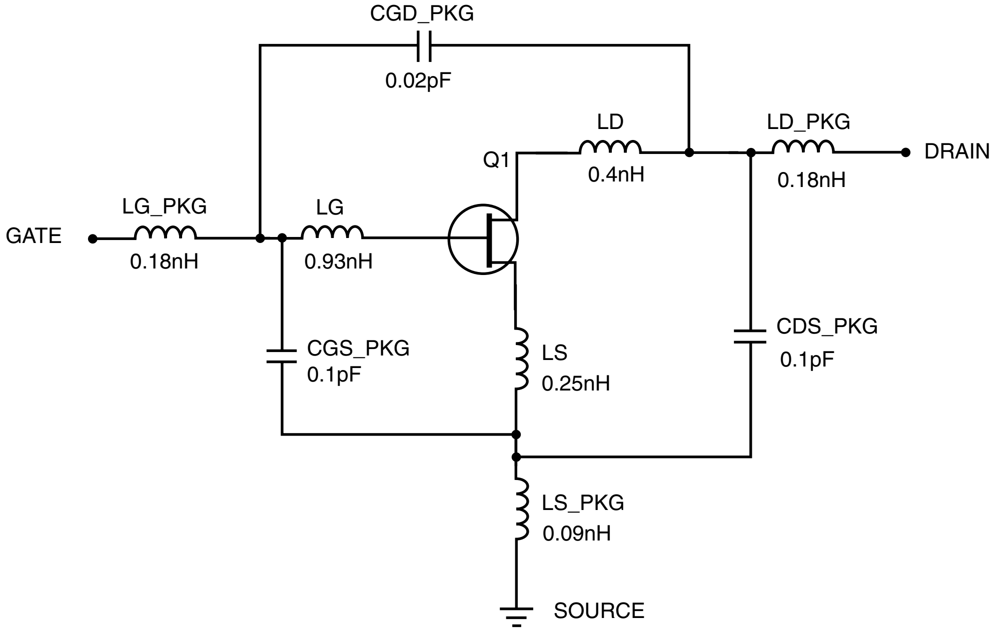
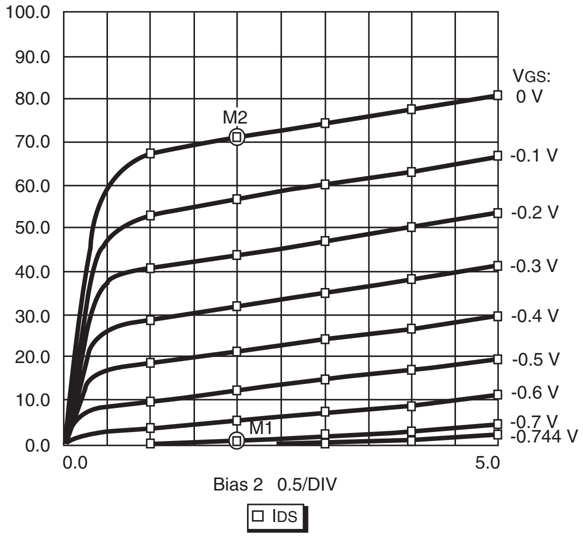


Fig. 1. NEC NE34018 Model Schematic

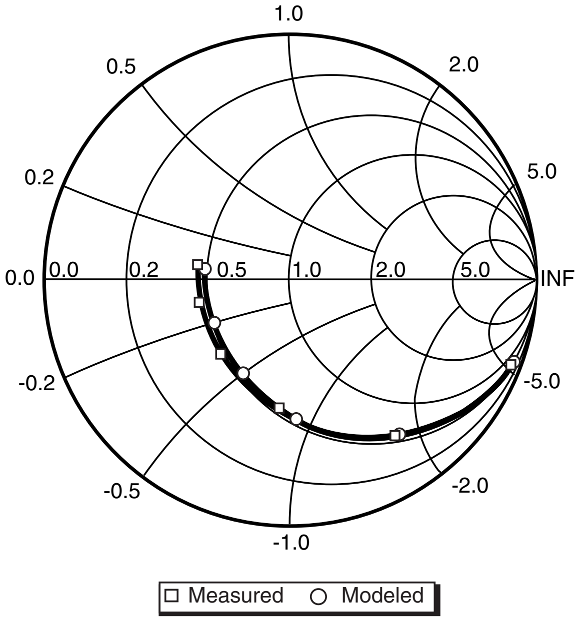
LIBRA PARAMETER	PARAMETER VALUE	DEFINITION
VTO	-0.6885	nonscaleable portion of the threshold voltage
VTOSC	0	scaleable portion of the threshold voltage
ALPHA	5	current saturation parameter
BETA	0.1838	transconductance parameter or coefficient
GAMMA	0.038	AC drain pull coefficient
GAMMADC	0.03	DC drain pull coefficient
Q	1.8	power law exponent
DELTA	0.25	output feedback coefficient
VBI	0.7	built-in gate potential
IS	3e-13	gate junction reverse saturation current
N	1	gate junction ideality factor
RIS	0	source end channel resistance
RID	0	drain end channel resistance
TAU	4e-12	transit time under gate
CDS	0.1e-12	drain-source capacitance
RDB	5000	dispersion source output impedance
CBS	1e-11	dispersion source capacitance
CGSO	0.95e-12	zero bias gate-source junction capacitance
CGDO	0.04e-12	zero bias gate-drain junction capacitance
DELTA1	0.3	capacitance saturation transition voltage parameter
DELTA2	0.05	capacitance threshold transition voltage parameter
FC	0.5	coefficient for forward bias depletion capacitance
VBR	infinity	gate-drain junction reverse bias breakdown voltage
RD	4	drain ohmic resistance
RG	1.5	gate ohmic resistance
RS	2	source ohmic resistance
RGMET	0	gate metal resistance
KF	0	flicker noise coefficient
AF	1	flicker noise exponent
XTI	3	temperature exponent for saturation current
EG	1.43	energy gap or band gap voltage
VTOTC	0	VTO temperature coefficient
BETATCE	0	BETA exponential temperature coefficient
FFE	1	flicker noise frequency exponent

Table 1. Triquint’s Own Model (TOM) Parameters for the NE34018



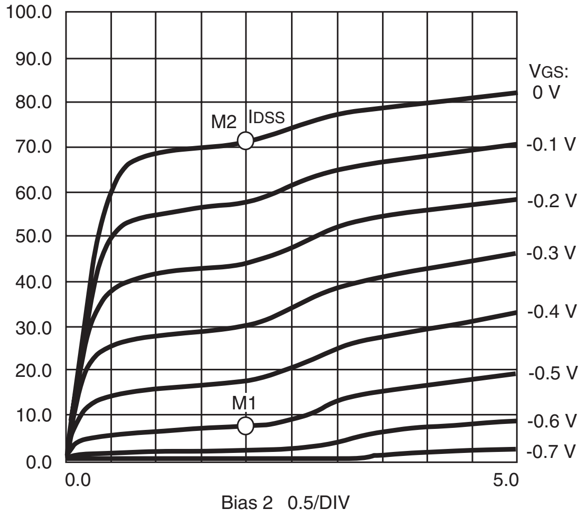
M1: V_{GS} = -0.744 V V_{DS} = 2 V I_{DS} = 100 µA
M2: V_{GS} = 0 V V_{DS} = 2 V I_{DSS} = 70.9 mA

Fig. 2a. NEC NE34018 Modeled I-V Curves



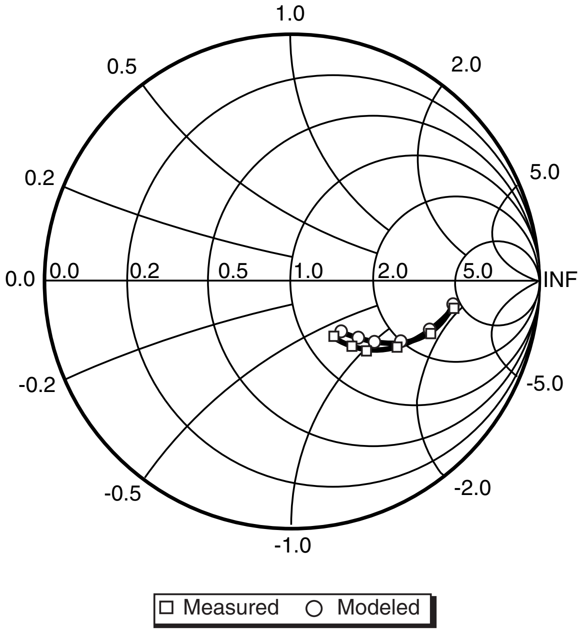
Frequency 0.5 to 6.0 GHz
V_{DS} = 3 V
I_D = 20 mA

Fig. 3. NEC NE34018 Measured vs. Modeled S11



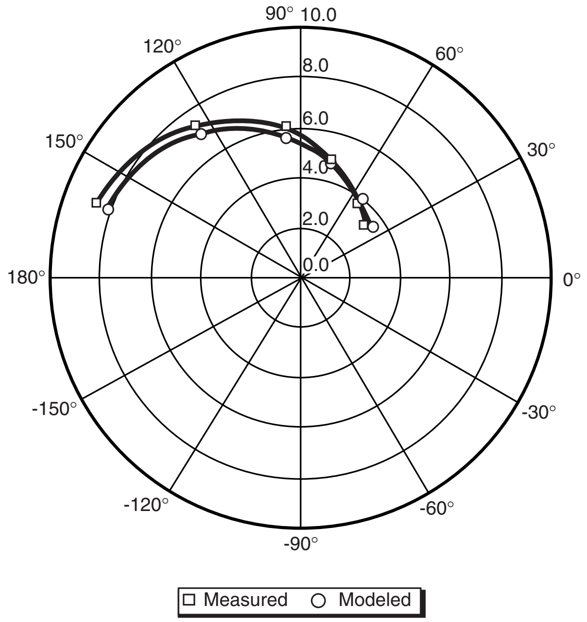
M1: V_{DS} = 2 V I_{DS} = 7.116 mA
M2: V_{DS} = 2 V I_{DSS} = 70.9 mA

Fig. 2b. NEC NE34018 Measured I-V Curves



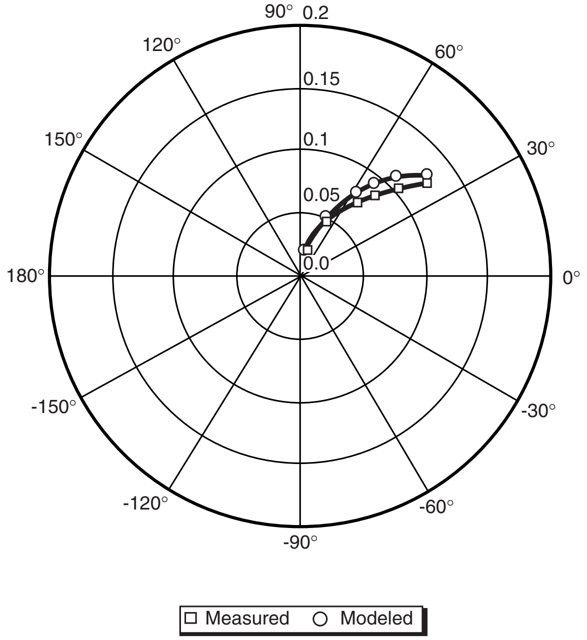
Frequency 0.5 to 6.0 GHz
V_{DS} = 3 V
I_D = 20 mA

Fig. 4. NEC NE34018 Measured vs. Modeled S22



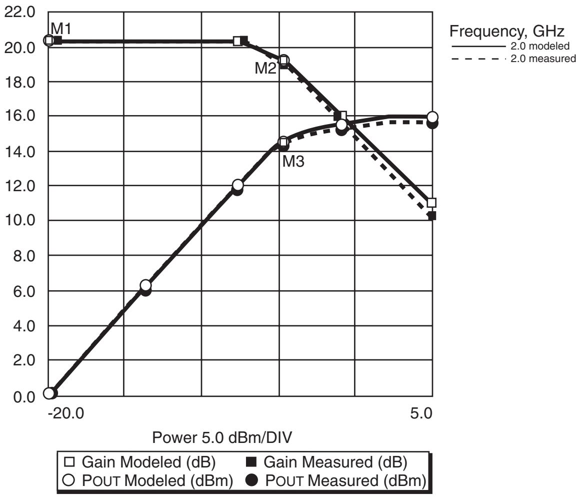
Frequency 0.5 to 6.0 GHz
V_{DS} = 3 V
I_D = 20 mA

Fig. 5. NEC NE34018 Measured vs. Modeled S21



Frequency 0.5 to 6.0 GHz
V_{DS} = 3 V
I_D = 20 mA

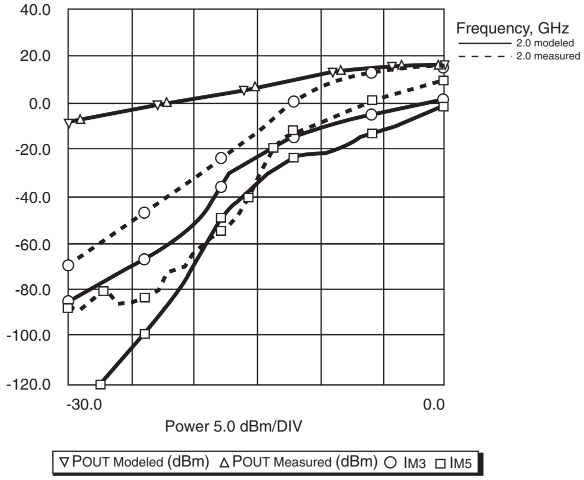
Fig. 6. NEC NE34018 Measured vs. Modeled S12



V_{DS} = 3 V I_D = 20 mA
Source Impedance: mag = 0.69 ang = 69.3
Load Impedance: mag = 0.54 ang = 24.4

M1: Power = -20.0 dBm Value = 20.2 dB
M2: Power = -4.75 dBm Value = 19.2 dB
M3: Power = -4.75 dBm Value = 14.5 dBm

Fig. 7. NEC NE34018 Measured vs. Modeled Gain and Power



V_{DS} = 3 V I_D = 20 mA
Source Impedance: mag = 0.69 ang = 69.3
Load Impedance: mag = 0.45 ang = 72.4

Fig. 8. NEC NE34018 Measured vs. Modeled Power, IM3 and IM5

Because nonlinear model results are predicted through the use of mathematical expressions which have been simplified from actual behavior, a nonlinear model can not perfectly predict the actual performance of the device being modeled. CEL sets a model performance target over the desired frequency and bias range of ±10% error from the measured data for the magnitude of the S-parameter predictions and ±10 degrees for the angle.

$$\text{error(magnitude)} = (|S11|\text{measured} - |S11|\text{modeled})/(|S11|\text{measured}) \tag{1}$$

$$\text{error(angle)} = \angle S11\text{measured} - \angle S11\text{modeled} \tag{2}$$

Fig. 9-16 present the final AC error data for the extracted NEC NE34018 model at the three biases representing the low (1V,5mA), middle (3V,20mA) and high (3V,40mA) bias ranges of the device.

Although the error target is ±10%, exceptions are made when actual differences in magnitudes are less than 0.1. For instance, a measured magnitude value of S22 = 0.27 and a modeled magnitude = 0.35, results in a error of 30% using equation (1), but the magnitude difference is only 0.08.

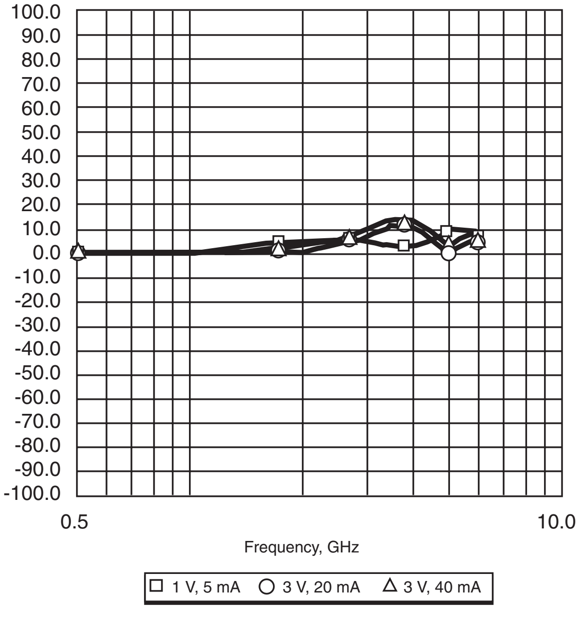


Fig. 9. NEC NE34018 Error Graph - Magnitude of S11

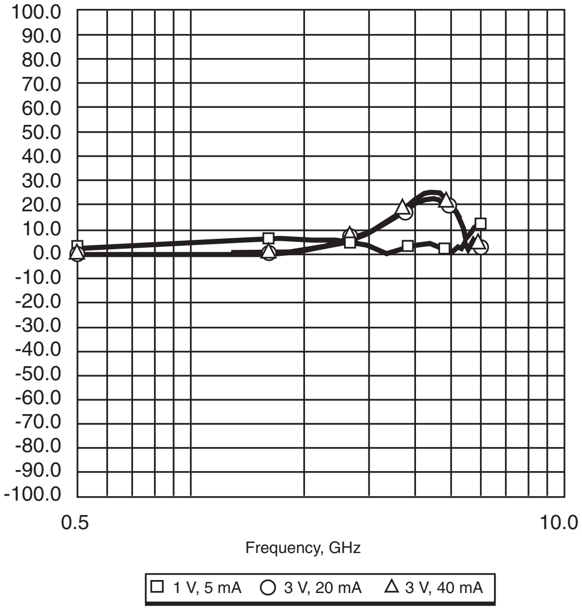


Fig. 10. NEC NE34018 Error Graph - Phase of S11

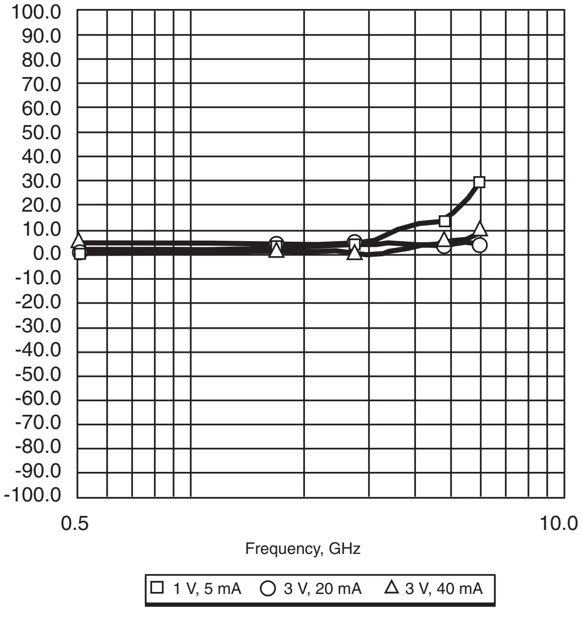


Fig. 11. NEC NE34018 Error Graph - Magnitude of S22

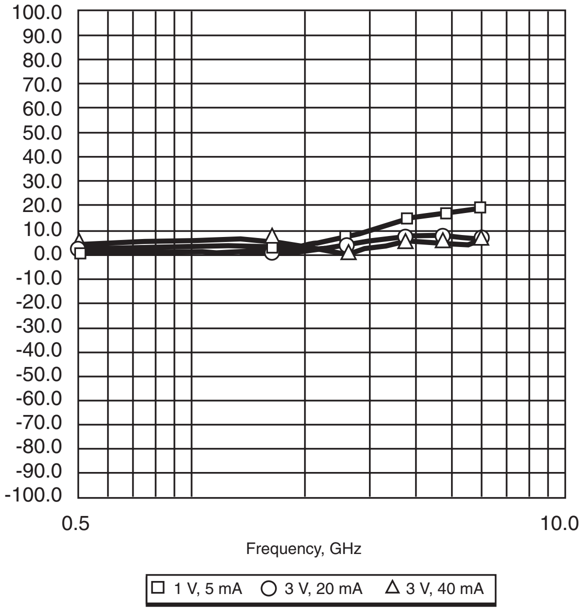


Fig. 12. NEC NE34018 Error Graph - Phase of S22

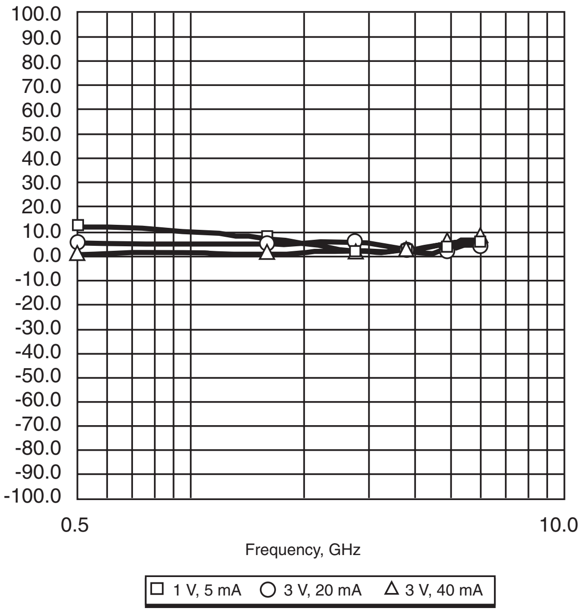


Fig. 13. NEC NE34018 Error Graph - Magnitude of S21

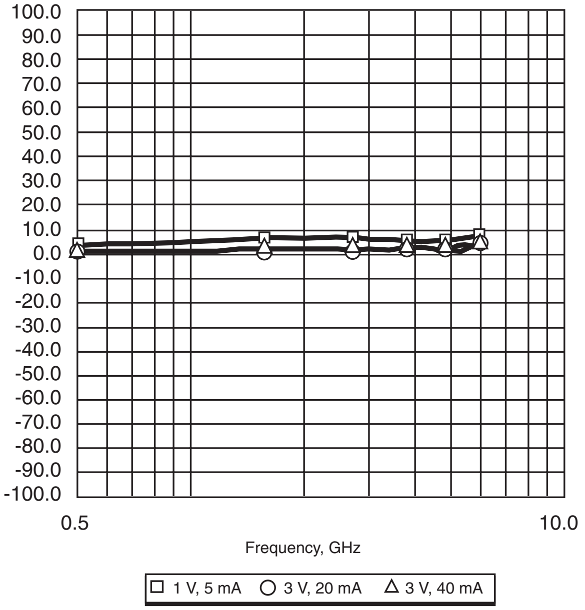


Fig. 14. NEC NE34018 Error Graph - Phase of S21

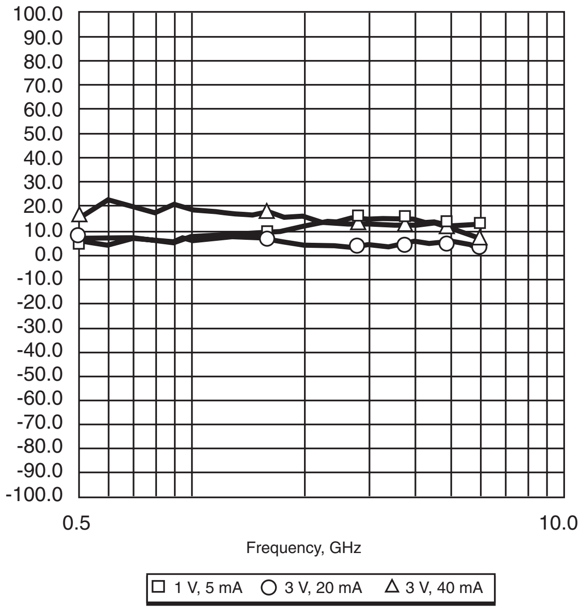


Fig. 15. NEC NE34018 Error Graph - Magnitude of S12

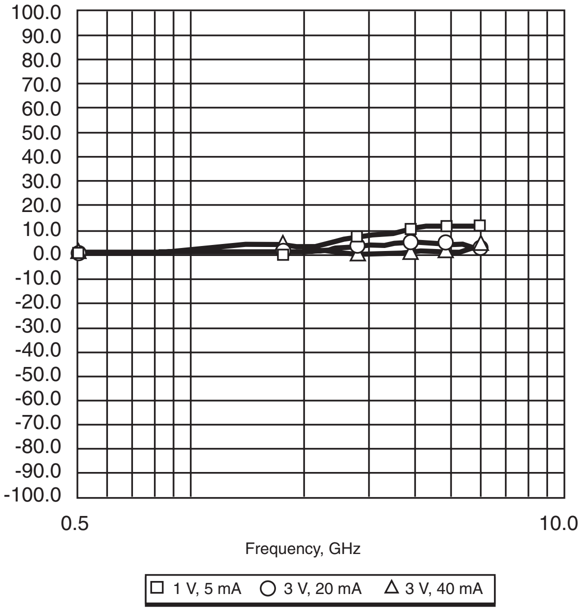


Fig. 16. NEC NE34018 Error Graph - Phase of S12

VII. Application circuit verification

Once the nonlinear device model has been extracted and accurately predicts measured data, how well can it predict actual circuit behavior? This question can be answered by building a circuit and comparing the measured performance to the simulated performance using the nonlinear model. A PCS amplifier was designed [2], built and tested. The design goals for the amplifier were:

Bias: Vds = 3V, Id = 20mA
Frequency: 1.932 - 1.99GHz (tested at 1.96GHz)
Noise figure: maximum of 0.8 dB
Output return loss: minimum of -15 dB

To achieve a realistic circuit simulation, the circuit elements and microstrip lines must be properly modeled in addition to having an accurate nonlinear model. The quality factor (Q) and the frequency at which it is defined (F) can be obtained from the component manufacturer for capacitors and inductors. Knowing the board material provides information needed to model the microstrip lines. Grounding and biasing must also be accurately represented in the simulation. Fig. 17-18 are HP-EEsof Series IV Libra schematic representations of the PCS amplifier used for simulation.

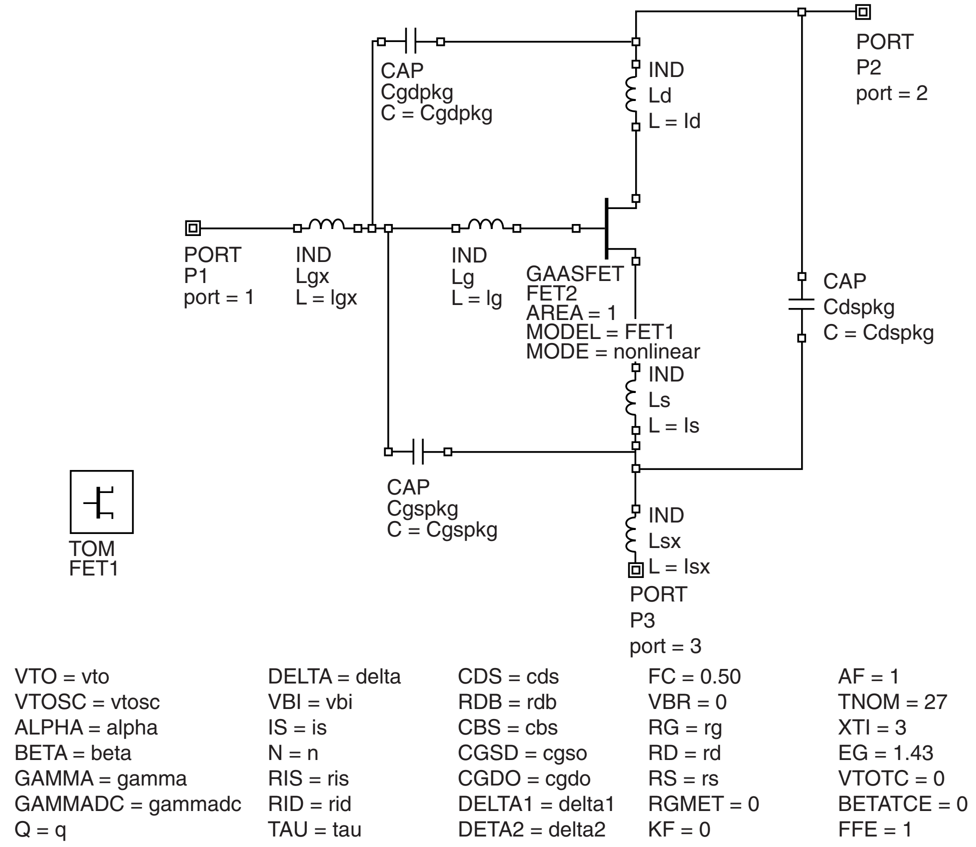


Fig. 17. HP-EEsof Series IV Libra NE34018 Schematic

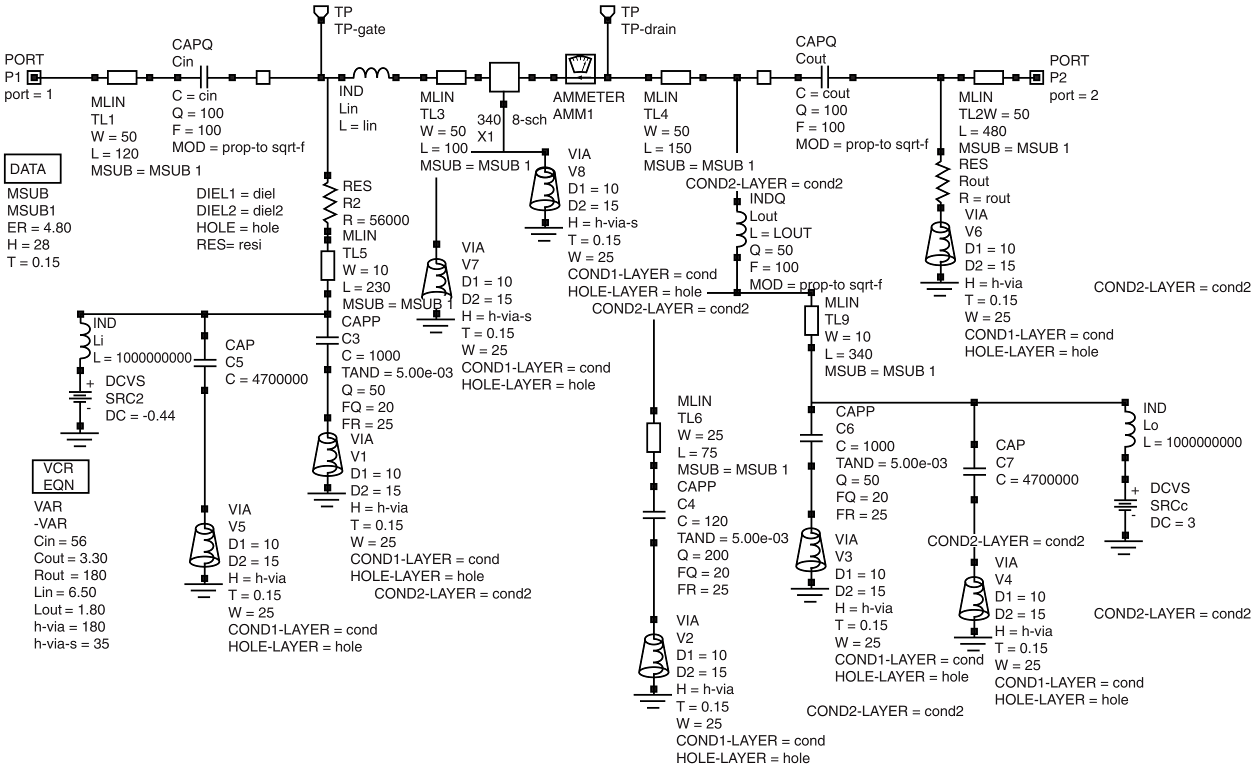
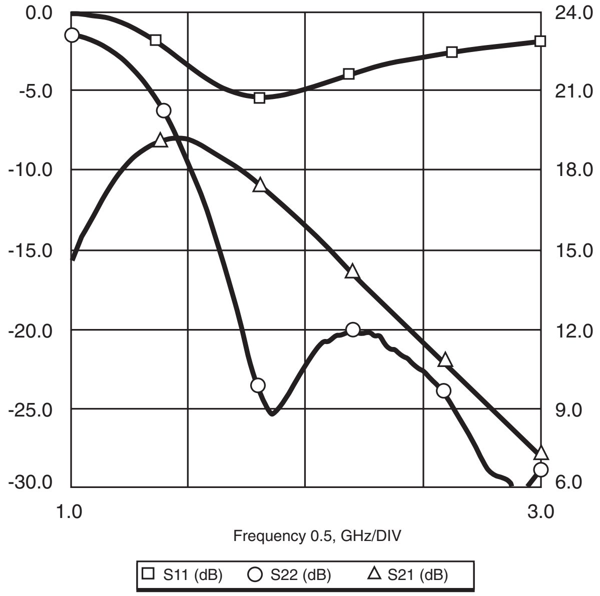


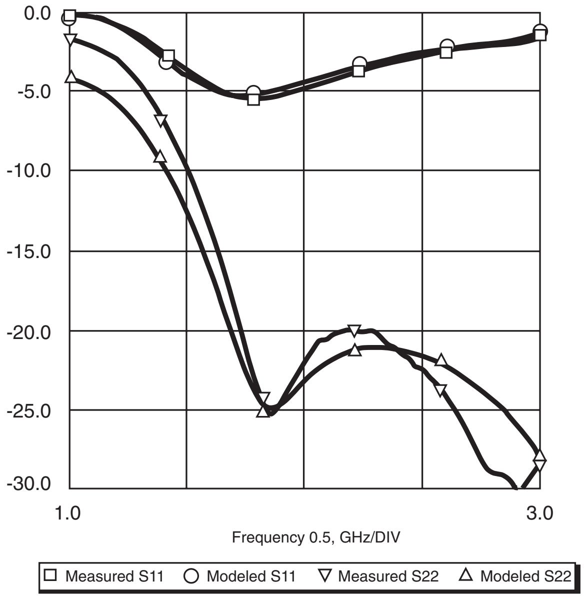
Fig. 18. HP-EEsof Series IV Libra LNA Schematic using the NE34018 Model

Fig. 19-24 illustrate how well the nonlinear model and appropriately modeled circuit elements can represent actual circuit behavior. For a low noise amplifier, the noise figure (Fig. 24) and the gain (Fig. 22) are key performance indicators.



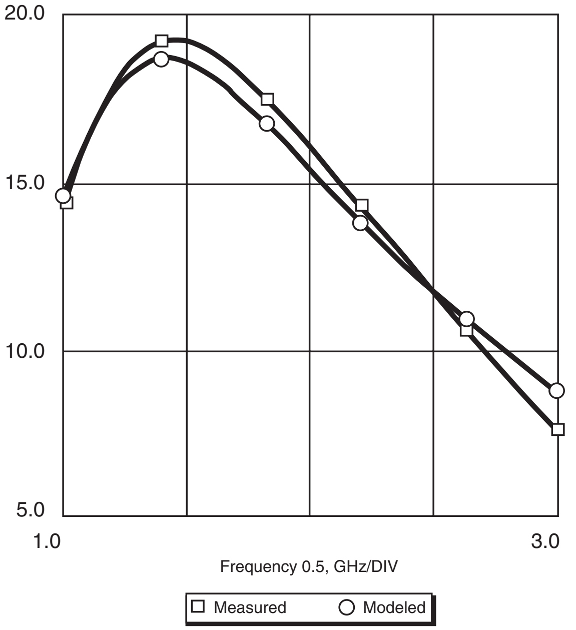
$V_{DS} = 3$ V
$I_D = 20$ mA

Fig. 19. LNA Measured S11, S22 and S21



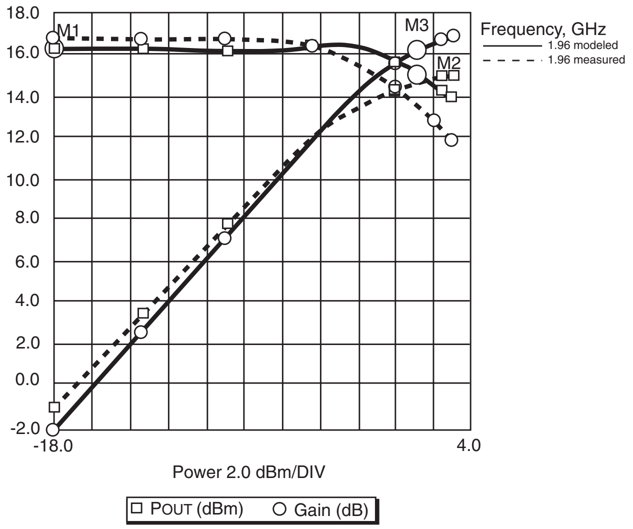
$V_{DS} = 3$ V
$I_D = 20$ mA

Fig. 20. LNA Measured vs. Modeled S11 and S22



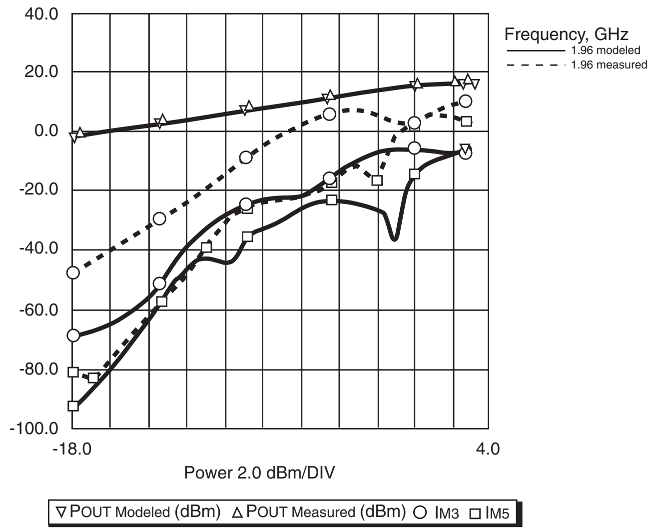
S21
VDS = 3 V
ID = 20 mA

Fig. 21. LNA Measured vs. Modeled S21



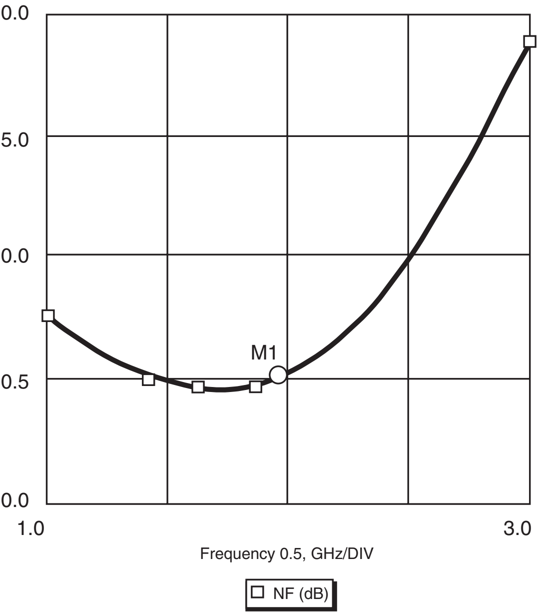
VDS = 3 V	ID = 20 mA
M1: Power = -18.0 dBm	Value = 16.1 dB
M2: Power = 1.4 dBm	Value = 15.1 dB
M3: Power = -4.75 dBm	Value = 16.5 dBm

Fig. 22. LNA Measured vs. Modeled Gain and Power



POUT, IM3 and IM5
VDS = 3 V ID = 20 mA

Fig. 23. LNA Measured vs. Modeled Power, IM3 and IM5



NF
VDS = 3 V
ID = 20 mA
M1 Frequency = 1.96 GHz
NF = 0.505 dB

Fig. 24. LNA Modeled NF

VIII. Conclusions

A nonlinear model is useful to predict and optimize the nonlinear performance of a design.

A nonlinear device model was extracted for the NE34018, and the results of the model generated data were compared to the measured data with good correlation.

The device model was further verified by using it in a PCS amplifier design and comparing the results of the simulation to data measured on the circuit, again with good correlation.

Acknowledgment

The authors would like to thank Bernie Urborg at California Eastern Laboratories for measurements on the device and the circuit.

References

[1] AN1023 “Converting GaAs FET Models for Different Nonlinear Simulators”, California Eastern Laboratories
[2] AN1022 “Designing Low Noise Amplifiers for PCS Application”, California Eastern Laboratories

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