APPLICATION NOTE

AN1032
Microwave Power GaAs Device Thermal Resistance Basics

1-INTRODUCTION

The operating temperature of GaAs power devices affects their reliability and RF performance. Since the majority of GaAs power microwave device failures occur in the channel (FETs) or junction (HBTs) area, all life-test data is referenced to the channel or junction temperature. In the following the term channel will be used for simplicity. The importance of accurately determining the channel temperature of each device cannot be overstressed. With a knowledge of the case or flange temperature, DC bias conditions, and RF power levels (P_{IN} and P_{OUT}), the channel temperature may be calculated using the thermal resistance of the device.

The problem for power amplifier designers who use GaAs devices is that the data sheet, in general, gives the device thermal resistance with the measurement conditions for only one set of conditions (case temperature and power dissipated or channel temperature). It doesn't give any information on calculating the device thermal resistance versus flange and channel temperature or power dissipated. A common error is to assume that the thermal resistance for GaAs devices is a constant and use that value for different device operating conditions. The thermal conductivity of GaAs material is a fairly strong function of temperature, which means that the channel and case or flange temperatures should be considered in order to calculate the thermal resistance of GaAs devices.

The purpose of this application note is to give the power amplifier designers a simple methodology to accurately calculate the device thermal resistances versus their operating temperatures from the data sheet information.

2-DEFINITION OF THERMAL IMPEDANCE (R_{TH})

The thermal resistance (R_{TH}) may be used to compute the channel temperature of a device under a given set of operating conditions, i.e., case or flange temperature (T_F), DC bias, and RF input and output power levels.

Thermal resistance, illustrated in Figure 1, defined as:

$$R_D = (T_{CH}-T_F)/P_D \qquad \text{(Eq. 2-1)}$$

where:
R_D is the channel-to-flange device thermal resistance (K/W or °C/W)
T_{CH} is the channel temperature (K or °C)
T_F is the case or flange temperature (K or °C)
P_D is the power dissipated by the device, which is equal to the DC input power plus RF input power minus RF output power ($P_D = V_{DS} \times I_{DS} + P_{IN} - P_{OUT}$) (W)

3-THERMAL CIRCUIT

Heat flow can be analyzed with a thermal circuit in the same way that current flow can be analyzed with an electrical circuit. In Fig. 2 the dissipated power (P_D) is analogous to a current-source driver, temperatures are analogous to voltages, and each element in the thermal path has a thermal resistance (R_{TH}) associated with it. The first element in the heat flow path is the channel-to-chip-bottom R_{TH} (R_C). The second element not shown in fig. 2 is the back side gold metalization (Au plated heat sink) of the chip Rth (R_{Au}). The third element is the solder (interface chip-to-case) R_{TH} (R_S). The fourth

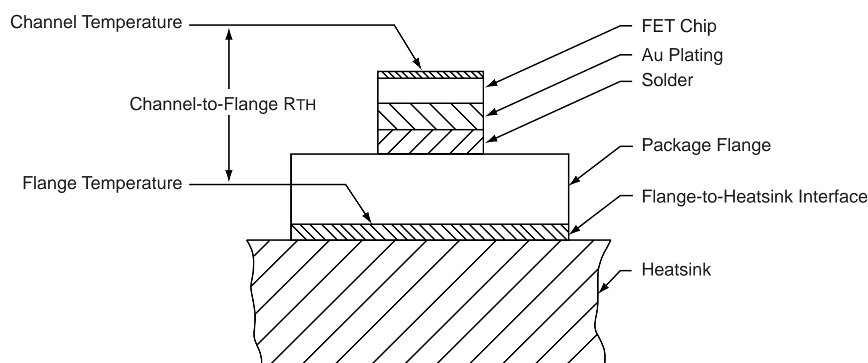

Figure 1. Power FET Channel-to-Flange Thermal Resistance.

element is the case or flange R_{TH} (R_F) . The next element is the Rth associated with mounting the device on the heat sink (R_I). The last element in the circuit shown is the heat sink-to-ambient R_{TH} (R_H).

The channel-to-flange R_{TH} of the device alone (R_D) which is given in the device data sheet consists of three practically constant R_{TH} versus temperature, R_{Au}, R_S & R_F , and the R_{TH} of the GaAs chip, R_C, which is a function of the temperature of the channel (T_{CH}) and the temperature of the chip bottom (T_{CB}):

$$R_D=R_F+R_S+R_{Au}+R_C(T_{CH},T_{CB}) \qquad (Eq.\ 3\text{-}1)$$

4-CASE OR FLANGE THERMAL RESISTANCE

For the case of power GaAs devices, the chips are long and narrow and the thermal resistance of the flange can be approximated with the following formula:

$$R_F= [L_N (16\ t/\pi\ W)]/(\pi\ \sigma_F\ N\ L) \qquad (Eq.\ 4\text{-}1)$$

where:
L_N is the natural logarithm (or $\log_e$)
R_F is the case or flange thermal resistance (K/W)
L is the length of the chip (cm)
σ_F is the thermal conductivity of the flange material (W/cm.K)
t is the flange thickness (cm)
W is the width of the chip (cm)
N is the number of chips used in the device

If these parameters cannot be obtained by the amplifier designer from the device supplier, the following assumption for power devices can be made:

$$R_F=0.3\ R_D \qquad (Eq.\ 4\text{-}2)$$

where:
R_D is the channel-to-flange device thermal resistance given in the data sheet.

5-CHIP BACK SIDE METALIZATION AND SOLDER THERMAL RESISTANCE

The thermal resistance of the chip back side metalization (R_{Au}) is very low due to gold good thermal conductivity and the relative thin layer (2 to 30 um). This R_{TH} can be disregarded for our purpose.

When the chips are correctly mounted to the flange (no voids underneath the chips), the interface chip-to-flange thermal resistance (R_S) is low in comparison with the flange and chip R_{TH} and can be ignored. It is about 2 to 3 % of the global device thermal resistance (R_D).

If needed it can be approximated by assuming uniform heat flow through the interface chip-to-flange:

$$R_S=t\ /\ (\sigma_S\ N\ L\ W) \qquad (Eq.\ 5\text{-}1)$$

where:
t is the solder thickness (cm)
σ_S is the solder thermal conductivity (W/cm.K)
N is the number of chips
L is the chip length (cm)
W is the chip width in (cm)

If these parameters cannot be obtained by the amplifier designer from the device supplier, the following assumption for power devices can be made:

$$R_S=0.025\ R_D \qquad (Eq.\ 5\text{-}2)$$

The value of these parameters (R_{Au} and R_S) will be assumed to be negligible for the rest of this application note.

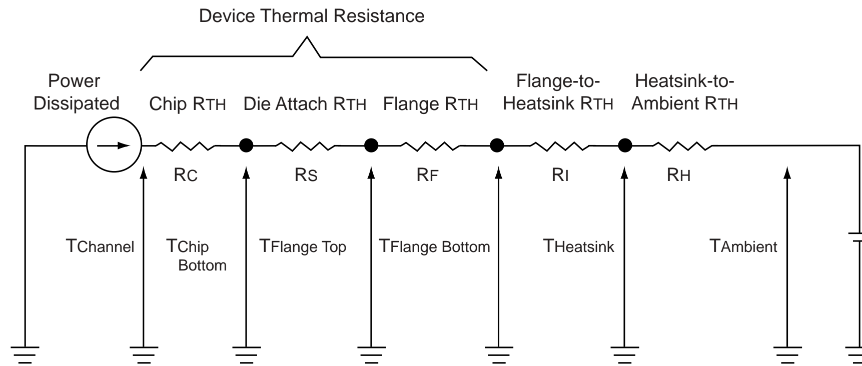

Figure 2. Thermal Circuit.

6-CHIP THERMAL RESISTANCE VERSUS TEMPERATURE

The thermal conductivity of the GaAs material can be expressed[1,2] by:

$$\sigma_{GaAs}=0.44\ [(T+273.2)/300]^{-1.25} \qquad \text{(Eq. 6-1)}$$

where:
σ_{GaAs} is the GaAs substrate thermal conductivity at T (W/cm.K)
T is the temperature of the GaAs substrate (°C)

From this Eq. 6-1 and the Kirchhoff's transformation the following formula can be derived (see appendix A):

$$R_{C2}=R_{C1}\ A/B \qquad \text{(Eq. 6-2)}$$

where:

$$A=[(T_{CH1}+273.2)^{-0.25}-(T_{CB1}+273.2)^{-0.25}]\ /\ (T_{CH1}-T_{CB1})$$

$$B=[(T_{CH2}+273.2)^{-0.25}-(T_{CB2}+273.2)^{-0.25}]\ /(T_{CH2}-T_{CB2})$$

R_{C1} is the chip thermal resistance for a chip bottom temperature T_{CB1} and a channel temperature T_{CH1} (°C/W or K/W)

R_{C2} is the chip thermal resistance for a chip bottom temperature T_{CB2} and a channel temperature T_{CH2} (°C/W or K/W)

T_{CH1} and **T_{CH2}** are the channel temperatures (°C)

T_{CB1} and **T_{CB2}** are the chip bottom temperatures (°C)

From the known thermal resistance (R_{C1}) of the chip for one set of temperatures (T_{CH1}, T_{CB1}), its thermal resistance (R_{C2}) can be calculated for any set of temperatures (T_{CH2}, T_{CB2}).

7-Methodology to Calculate Device Thermal Resistance versus Temperature from the Data Sheet Information (Fig. 3 shows the flow chart of this methodology)

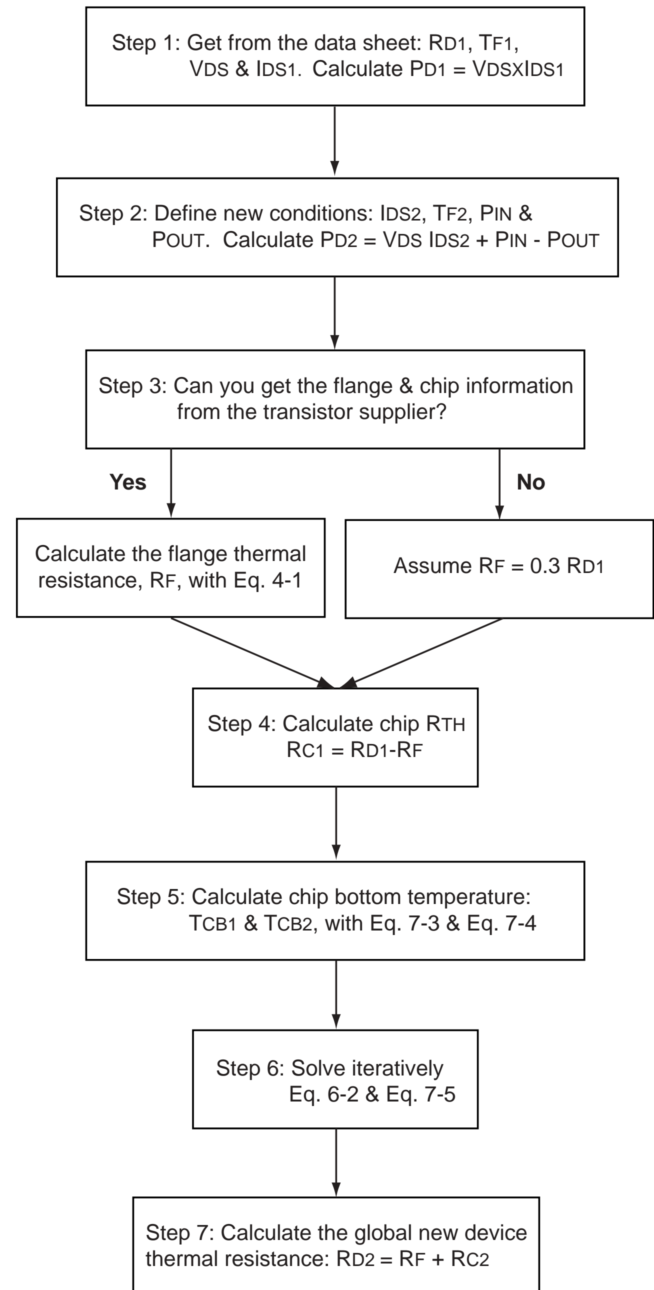

Figure 3. Thermal Resistance Calculation.

Step 1: get R_{C1}, T_{F1} and P_{D1} from the data sheet

Get the value of the device thermal resistance (R_{D1}) for a defined set of conditions from the data sheet. The measurement conditions are in general without RF. The drain-to-source voltage (V_{DS}) and the drain current (I_{DS1}) or the power dissipated ($P_{D1}=V_{DS}\ I_{DS1}$) are given.

Step 2: calculate P_{D2} from the new operating conditions

The new conditions are defined by the application: I_{DS2}, T_{F2}, P_{IN} & P_{OUT}.

The power dissipated is:

$$P_{D2}=V_{DS}\ I_{DS2}+P_{IN}-P_{OUT} \qquad \text{(Eq. 7-1)}$$

where:
V_{DS} is the drain voltage (V)
I_{DS2} is the drain current (A)
P_{IN} is the input power (W)
P_{OUT} is the output power (W)

Remark:
V_{DS} is assumed to be the same as the one defined in the data sheet because R_D is a function of V_{DS}.

Step 3: calculate the flange thermal resistance (R_F)

From the device supplier or from measurement and literature get the flange thickness (t), and thermal conductivity (σ_F), the chip width (W) and length (L), the number of chips (N) used and use Eq. 4-1 to calculate the flange thermal resistance (R_F).

If these parameters cannot be obtained from the device supplier or measured use Eq. 4-2:

Step 4: calculate the chip thermal resistance for T_{F1} and T_{CH1}

$$R_{C1}=R_{D1}-R_F \qquad \text{(Eq. 7-2)}$$

Step 5: calculate the chip bottom temperatures

$$T_{CB1}=T_{F1}+R_F P_{D1} \qquad \text{(Eq. 7-3)}$$
$$T_{CB2}=T_{F2}+R_F\ P_{D2} \qquad \text{(Eq. 7-4)}$$

Step 6: new chip thermal resistance (R_{C2}) and channel temperature (T_{CH2})

The following set of equations has to be solved:

$$R_{C2}=R_{C1}\ A/B \qquad \text{(Eq. 6-2)}$$

where:

$$A=[(T_{CH1}+273.2)^{-0.25}-(T_{CB1}+273.2)^{-0.25}] / (T_{CH1}-T_{CB1})$$
$$B=[(T_{CH2}+273.2)^{-0.25}-(T_{CB2}+273.2)^{-0.25}] / (T_{CH2}-T_{CB2})$$

and

$$T_{CH2}=T_{CB2}+R_{C2}\ P_{D2} \qquad \text{(Eq. 7-5)}$$

It can be solved by using an iterative method. The nth approximation of the chip thermal resistance, $R_{C2/n}$, and the channel temperature, $T_{CH2/n}$, are obtained respectively from Eq. 6-2 and Eq. 7-5 in the nth step by using the previous approximation of $R_{C2/n-1}$ and $T_{CH2/n-1}$ obtained in the $n-1^{th}$ step.

The initial assumed values of R_{C2} and T_{CH2} for starting the first iteration, n=1, are respectively $R_{C2/0}=R_{C1}$ and $T_{CH2/0}=T_{CB2}+R_{C1}\ P_{D2}$.

From the set of values, R_{C1}, T_{CB1}, T_{CH1}, T_{CB2} and $T_{CH2/n-1}$ and Eq. 6-2, calculate the nth approximation of $R_{C2/n}$. Then calculate the nth approximation of $T_{CH2/n}$ from Eq. 7-5.

If the following double inequality is satisfied, $-0.01<(R_{C2/n}-R_{C2/n-1})/R_{C2/n-1}<0.01$ stop the iteration process, $R_{C2}=R_{C2/n}$ and $T_{CH2}=T_{CH2/n}$

If this double inequality is not satisfied, then perform a $n+1^{th}$ iteration with the same process.

A small program may be written to solve this system of equations iteratively (see Appendix B) or, because this sequence converges to the solution rapidly (two to three iterations), a simple calculator with an exponential function may be used.

The graphical plot in Fig. 4 may also be used to calculate R_C from Eq. 6-2. The plot represents the normalized chip thermal resistance, $K_C=R_C/R_{CO}$, R_{CO} being the chip thermal resistance for T_{CHO}=140°C and T_{CBO}=20°C, versus T_{CH} and T_{CB}. To determine R_{C2} from the graphical plot Fig. 4, proceed as follows: first get $K_{C1}=R_{C1}/R_{CO}$ for T_{CB1} and T_{CH1}, then get $K_{C2}=R_{C2}/R_{CO}$ for T_{CB2} and T_{CH2}. The new thermal resistance value at T_{CB2} and T_{CH2} is given by the equation $R_{C2}=R_{C1}\ K_{C2}/K_{C1}$.

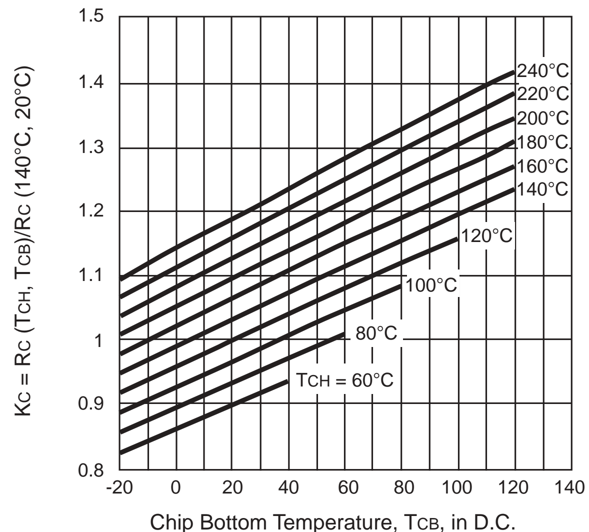

Figure 4. GaAS FET Chip R_{TH} vs. Channel & Chip Bottom Temperature.

Step 7: Calculate R_{D2}

The new device Channel-to-flange thermal resistance at T_{CB2}, T_{CH2} is:

$$R_{D2}=R_F+R_{C2} \qquad \textit{(Eq. 7-6)}$$

Example 1
Step 1:

The data sheet gives the following information:
R_{D1}=1.04 K/W at T_{F1}=25°C, V_{DS}=10.0 V and I_{DSQ1}=6.0 A
The power dissipated is: P_{D1}=10.0x6.0=60.0 W

Step 2:

This device is used for a reliability test at T_{F2}=150°C with a power dissipated P_{D2}= 60 W. Its thermal resistance needs to be known for these new operating conditions to calculate the device channel temperature.

Step 3:

The flange and chip parameters are unknown, we assumed in this case that:
R_F=0.3 R_{D1}=0.3x1.04=0.312 K/W

Step 4:

The chip thermal resistance is: R_{C1}=1.04-0.312=0.728 K/W

Step 5:

The chip bottom temperatures are:
T_{CB1}=25+0.312x60= 43.7°C
T_{CB2}=150+0.312x60=168.7°C

Step 6:

First iteration
From Eq. 6-2 and R_{C1}=0.728 K/W, T_{CB1}=43.7°C, T_{CH1}=25+1.04x60=87.4°C, T_{CB2}=168.7°C, $T_{CH2/0}$=168.7+0.728x60=212.4°C, calculate $R_{C2/1}$: $R_{C2/1}$=1.08 K/W, which corresponds to a difference of 48 % from the initial assumed value. A second iteration is necessary.

Second iteration
Perform a second iteration with $T_{CH2/1}$=168.7+1.08x60= 233.5 °C, which gives: $R_{C2/2}$=1.109 K/W which corresponds to a difference of 2.7 % from the assumed value $R_{C2/1}$. A third iteration is necessary.

Third iteration
Perform a third iteration with $T_{CH2/2}$=168.7+1.11x60= 235.2 °C, which gives: $R_{C2/3}$=1.111 K/W which corresponds to a difference of 0.2 % from the assumed value $R_{C2/2}$. A forth iteration is not needed.

Step 7:

The new device thermal resistance is: R_{D2}=1.111+0.312= 1.423 K/W and T_{CH2}=168.7+1.111x60=235.4°C

If the original value, R_{D1}, were used it would introduce an error of -23.0°C for the channel temperature.

Example 2
Step1:

The data sheet gives the following information: R_D= 0.66 K/W at T_{F1}=65°C, V_{DS}=10.0 V and I_{DS1}=12.0 A. The power dissipated is: P_{D1}=10.0x12.0=120.0 W

Step 2:

This device is used at T_{F2}=20°C and with P_{IN}=3.0 W, P_{OUT}=60.0 W, I_{DS2}=15 A, V_{DS}=10.0 V. The power dissipated is: P_{D2}=15.0x10.0+3.0-60.0=93.0 W

Step 3:

The flange is 0.178 cm thick and made of Cu/W-15 material with a thermal conductivity of 1.90 W/cm.K. Four chips are used and each chip is 0.42 cm long and 0.10 cm wide. From Eq.4-1, the flange thermal resistance can be calculated: R_F=0.220 K/W

Step 4:

The chip thermal resistance is: R_{C1}=0.660-0.220=0.440 K/W

Step 5:

The chip bottom temperatures are:
T_{CB1}=65+0.220x120=91.4°C
T_{CB2}=20+0.220x93=40.5°C

Step 6:

First iteration
From Eq. 6-2 and R_{C1}=0.440 K/W, T_{CB1}=91.4°C, T_{CH1}=91.4+0.440x120=144.2°C, T_{CB2}=40.5°C, $T_{CH2/0}$=40.5+0.440x93=81.4°C, calculate $R_{C2/1}$: $R_{C2/1}$= 0.362 K/W, which corresponds to a difference of -18 % from the previous assumed value. A second iteration is needed.

Second iteration
Perform a second iteration with $T_{CH2/1}$=40.5+0.362x93= 74.2 °C, which gives: $R_{C2/2}$=0.357 K/W which corresponds to a difference of -1.4 %. A third iteration is needed.

Third iteration
Perform a third iteration with $T_{CH2/2}$=40.5+0.357x93= 73.7 °C, which gives: $R_{C2/3}$=0.357 K/W which corresponds to a difference of 0.1 %. A new iteration is not needed.

Step 7:

The new device thermal resistance is: R_{D2}=0.357+0.220= 0.577 K/W

If the original value, R_{D1}, were used it would introduce an error of 7.5°C for the channel temperature.

Remarks:

Sometimes the following formula is used to calculate device R_{TH} versus channel temperature

$R_{D2}=R_{D1}\,(T_{CH2}/T_{CH1})^{-1.25}$

where:
T_{CH2} and T_{CH1} are the channel temperature in K

This is correct only if the $T_{CB1}=T_{CH1}$ and $T_{CB2}=T_{CH2}$, in other terms if $P_{D1}=P_{D2}=0$ W, which is rarely the case.

This formula doesn't take into account that the flange R_{TH} which is constant versus temperature and has first to be subtracted from R_{D1} before applying any temperature correction.

APPENDIX A

GaAs Chip Thermal Resistance versus Temperature

GaAs Material Thermal Conductivity versus Temperature

The thermal conductivity of GaAs material is a function of the temperature and can be expressed by the following formula[1,2]:

$$\sigma_{GaAs}=A\,T^{n} \qquad \text{(Eq. A-1)}$$

where:
σ_{GaAs} is the GaAs material thermal conductivity at the temperature T (W/cm.K)
T is the GaAs material temperature (K)
n=-1.25

The dependence of σ_{GaAs} on the doping density is neglected because the regions where the material is doped are negligibly thick compared to the dimensions over which the heat is spread.

Kirchhoff's Transformation

The temperature dependence of the thermal conductivity of the GaAs chip can be taken into account by using the Kirchhoff's transformation. The method consists of solving the heat-flow equation, analytically, numerically, or empirically under the boundary conditions of usual interest. Then Kirchhoff's transformation immediately yields the nonlinear steady-state temperature rise or thermal resistance of an uniform heat sink of any shape with no further approximations and negligible further effort.

At each point x of the conductor a fictitious linearized temperature $\alpha(x)$ is associated with the actual temperature T(x) with the formula[3]:

$$\alpha(x)=T_O+\sigma_O^{-1}\int_{T_O}^{T}\sigma(T)\,dT \qquad \text{(Eq. A-2)}$$

where $\sigma_O=\sigma(T_O)$ is the thermal conductivity at $T=T_O$.

Chip Thermal Resistance Versus Temperature

Substituting the expression of σ from Eq. A-1 into Eq. A-2 and solving for the linearized channel temperature corresponding to chip bottom temperature T_{CB1} and channel temperature T_{CH1}:

$$\alpha_1=\alpha(T_{CB1},T_{CH1})=T_{CB1}+(A\,T_{CB1}^{n})^{-1}\int_{T_{CB1}}^{T_{CH1}}A\,T^{n}\,dT$$

$$=T_{CB1}+T_{CB1}^{-n}\,[T^{n+1}/(n+1)]_{T_{CB1}}^{T_{CH1}}$$

$$\alpha_1=T_{CB1}+[(n+1)T_{CB1}^{n}]^{-1}(T_{CH1}^{n+1}-T_{cb1}^{n+1}) \qquad \text{(Eq. A-3)}$$

Using the definition of the thermal resistance given in Eq. 1-1 to solve for the linearized channel temperature we get:

$$\alpha_1=T_{CB1}+R\,(\alpha_1)\,P_{D1} \qquad \text{(Eq. A-4)}$$

where $R(\alpha_1)$ is the linearized thermal resistance corresponding to the linearized channel temperature α_1. This is the value which the thermal resistance would have if the thermal conductivity of the GaAs material did not vary with temperature and was $\sigma(T)=\sigma(T_{CB1})$. We may express $R(\alpha_1)$ as:

$$R\,(\alpha_1)=G/\sigma(T_{CB1})=G\,T_{CB1}^{-n}/A \qquad \text{(Eq. A-5)}$$

where $\sigma(T_{CB1})$ is equal to the thermal conductivity of the material at a temperature of T_{CB1} [$\sigma(T_{CB1})=AT_{CB1}^{\,n}$], and G is a factor depending on the device geometry.

Substituting $R(\alpha_1)$ from Eq. A-5 into Eq. A-4:

$\alpha_1=T_{CB1}+P_{D1}\,G\,T_{CB1}^{-n}/A$ solving for P_{D1}

$$P_{D1}=(\alpha_1-T_{CB1})A\,T_{CB1}^{n}/G \qquad \text{(Eq. A-6)}$$

We want to find the channel-to-chip-bottom thermal resistance at T_{CB1} and T_{CH1} defined as:

$$R_{C1}=(T_{CH1}-T_{CB1})/P_{D1} \qquad \text{(Eq. A-7)}$$

Substituting Pd1 from Eq. A-6 into Eq. A-7:

$$R_{C1}=G(T_{CH1}-T_{CB1})/[\,A\,T_{CB1}^{n}(\alpha_1-T_{CB1})] \qquad \text{(Eq. A-8)}$$

Substituting the expression of $\alpha 1$ from Eq. A-3 into Eq. A-8, we obtain after simplification:

$$R_{C1}=[G/A)]\ (n+1)(T_{CH1}-T_{CB1})/(\ T_{CB1}^{n+1}-T_{CB1}^{n+1})\ \text{(Eq. A-9)}$$

Similarly, for $T_{CH}=T_{CH2}$ and $T_{CB}=T_{CB2}$, R_{C2} can be calculated:

$$R_{C2}=[G/A]\ (n+1)(T_{CH2}-T_{CB2})/(\ T_{CH2}^{n+1}-T_{CB2}^{n+1})\ \text{(Eq. A-10)}$$

Dividing Eq. A-10 by Eq. A-9 and solving for R_{C2} we obtain:

$$R_{C2}=R_{C1}[(T_{CH1}^{n+1}-T_{CB1}^{n+1})/(T_{CH1}-T_{CB1})]/[(T_{CH2}^{n+1}-T_{CB2}^{n+1})/(T_{CH2}-T_{CB2})]\quad \text{(Eq. A-11)}$$

where:

R_{C2}: chip channel-to-chip bottom thermal resistance at chip bottom temperature T_{CB2} and at channel temperature T_{CH2} (K/W)

R_{C1}: chip channel-to-chip bottom thermal resistance at chip bottom temperature T_{CB1} and at channel temperature T_{CH1} (K/W)

T_{CB1} and **T_{CB2}:** are the chip bottom temperatures (K)

T_{CH1} and **T_{CH2}:** are the channel temperatures (K)

T in K=T in °C+273.2

n=-1.25

APPENDIX B

HP48X or GX Calculator Program to Calculate GaAs Device Thermal Resistances versus Temperature

Here is an example of a program for a HP48X or GX calculator to calculate the thermal resistance of GaAs devices versus temperature when this parameter is already known for one operating point.

Begin by creating a directory for RTH, then get into that directory.

1-Get subprograms

These following subprograms prompt the user to input a value for each of the following parameters:

RTH1 (device thermal resistance @ TF1 & TCH1 in K/W), TF1 (flange temperature in °C), TCH1 (channel temperature in °C), TF2 (flange temperature in °C), PD2 (power dissipated at TF2 & TCH2 in W), RF (flange thermal resistance in K/W) and n (n=-1.25).

<<“Key in RTH1 in K/W” “ ” INPUT OBJ—>‘RTH1’STO >>
ENTER ‘GetRTH1’ STO to put GetRTH in the stack and store the program GetRTH1.

<<“Key in TF1 in D.C.” “ ” INPUT OBJ—>‘ TF1’ STO >>
ENTER ‘GetTF1’ STO to put GetTF1 in the stack and store the program GetTF1.

<<“Key in TCH1 in D.C.” “ ” INPUT OBJ—>‘ TCH1’STO >>
ENTER ‘GetTCH1’ STO to put GetTCH1 in the stack and store the program GetTCH1.

<<“Key in TF2 in D.C.” “ ” INPUT OBJ—>‘ TF2’STO >>
ENTER ‘GetTF2’ STO to put GetRTF2 in the stack and store the program GetTF2.

<<“Key in PD2 in W” “ ” INPUT OBJ—> ‘ PD2’ STO >>
ENTER ‘GetPD2’ STO to put GetPD2 in the stack and store the program GetPD2 .

<<“Key in n” “ ” INPUT OBJ—> ‘ Expo’ STO >>
ENTER ‘Getn’ STO to put Getn in the stack and store the program Getn.

2-Compute subprograms

The compute subprograms handle the computational chores in the program.

<<‘RTH1’ RCL ‘RF’ RCL - ‘RC1’ STO ‘RC1’ RCL ‘RC2’ STO>>
ENTER ‘CompRC1’ STO to put CompRC1 in the stack and store it.

<<‘TCH1’ RCL ‘TF1’ RCL - ‘RTH1’ RCL / ‘PD1’ STO >>
ENTER ‘CompPD1’ STO to put CompPD1 in the stack and store it.

<<‘RF’ RCL ‘PD1’ RCL x ‘TF1’ RCL + ‘TCB1’ STO >>
ENTER ‘CompTCB1’ STO to put CompTBC1 in the stack and store it.

<<‘RF’ RCL ‘PD2’ RCL x ‘TF2’ RCL + ‘TCB2’ STO >>
ENTER ‘CompTCB2’ STO to put CompTCB2 in the stack and store it.

<<‘TCB2’ RCL ‘PD2’ RCL ‘RC2’ RCL x + ‘TCH2’ STO >>
ENTER ‘CompTCH2’ STO to put CompTCH2 in the stack and store it.

<< ‘Expo’ RCL —> a b c << ‘(((a+273.2)^(c+1))-((b+273.2)^(c+1))) / (a-b)’ EVAL —> NUM>> >>
ENTER ‘CompAorB’ STO to put CompAorB in the stack and store it.

<< ‘TCH1’ RCL ‘TCB1’ RCL CompAorB ‘TCH2’ RCL ‘TCB2’ RCL CompAorB ‘RC1’ RCL —> a b c <<‘axc/b’ EVAL —> NUM >> ‘RC2’ STO >>
ENTER ‘CompRC2’ STO to put CompRC2 in the stack and store it.

3-Label program

The final subprogram which adds a tag to the calculated RC2 value.

<< “RTH2 in K/W=“ —> TAG>>
ENTER ‘Label’ STO to put Label in the stack and store it

4-Main program (five iterations are performed to calculate RC2)

<< GetRTH1 GetTF1 GetTCH1 GetTF2 GetPD2 GetPD2 GetRF Getn CompPD1 CompRC1 CompTCB1

CompTCB2 1 5 START CompTCH2 CompRC2 NEXT 'RC2' RCL 'RF' RCL + Label >>
ENTER 'RCAL' STO to put Label in the stack and store it.

5-Running RCAL program

Run the RCAL program to find the Thermal Resistance of a device, RTH2, at TF2= 150°C and PD2= 60 W when its thermal resistance, RTH1, is known and is 1.04 K/W at TF1=25°C, and TCH1=87.4°C and knowing that its flange thermal resistance, RF, is 0.312 K/W.

Press RCAL

Program Prompt or Display	Your Action
Key in RTH1 (K/W)	1.04 ENTER
Key in TF1 (D.C.)	25 ENTER
Key in TCH1 (D.C.)	87.4 ENTER
Key in TF2 (D.C.)	150 ENTER
Key in PD2 (D.C.)	60 ENTER
Key in RF (K/W)	0.312 ENTER
Key in n	-1.25 ENTER
RTH2 in K/W= 1.423	

References

1. Robert Anholt, "Electrical and Thermal Characterization of MESFETs, HEMTs, and HBTs" Artech House, Boston.London, chapter 4, page 62.

2. P.D. Maycock, "Thermal Conductivity of Silicon, Germanium, III-V Compounds and Alloys", Solid-State Eletronics, Pergamon Press 1967. Vol. 10, pp. 161-168. Printed in Great Britain.

3. W.B. Joyce, "Thermal Resistance of Heat Sinks with Temperature-Dependent Conductivity", Solid-State Electronics, 1975, Vol. 18, pp. 321-322. Pergamon Press. Printed in Great Britain.

California Eastern Laboratories

Exclusive Agents for NEC RF, Microwave and Optoelectronic semiconductor products in the U.S. and Canada

4590 Patrick Henry Drive, Santa Clara, CA 95054-1817
Telephone 408-988-3500 • FAX 408-988-0279 •Telex 34/6393
Internet: http:/WWW.CEL.COM

Information and data presented here is subject to change without notice. California Eastern Laboratories assumes no responsibility for the use of any circuits described herein and makes no representations or warranties, expressed or implied, that such circuits are free from patent infingement.

© California Eastern Laboratories 02/20/2003