

# AN1030

## Microwave Power GaAs Device Thermal Resistance Basics

### 1-INTRODUCTION

The operating temperature of GaAs power devices affects their reliability and RF performance. Since the majority of GaAs power microwave device failures occur in the channel (FETs) or junction (HBTs) area, all life-test data is referenced to the channel or junction temperature. In the following the term channel will be used for simplicity. The importance of accurately determining the channel temperature of each device cannot be overstressed. With a knowledge of the case or flange temperature, DC bias conditions, and RF power levels (PIN and POUT), the channel temperature may be calculated using the thermal resistance of the device.

The problem for power amplifier designers who use GaAs devices is that the data sheet, in general, gives the device thermal resistance with the measurement conditions for only one set of conditions (case temperature and power dissipated or channel temperature). It doesn't give any information on calculating the device thermal resistance versus flange and channel temperature or power dissipated. A common error is to assume that the thermal resistance for GaAs devices is a constant and use that value for different device operating conditions. The thermal conductivity of GaAs material is a fairly strong function of temperature, which means that the channel and case or flange temperatures should be considered in order to calculate the thermal resistance of GaAs devices.

The purpose of this application note is to give the power amplifier designers a simple methodology to accurately calculate the device thermal resistances versus their operating temperatures from the data sheet information.

### 2-DEFINITION OF THERMAL IMPEDANCE (RTH)

The thermal resistance (RTH) may be used to compute the channel temperature of a device under a given set of operating conditions, i.e., case or flange temperature (TF), DC bias, and RF input and output power levels.

Thermal resistance, illustrated in Figure 1, defined as:

$$R_D = (T_{CH} - T_F) / P_D \quad (Eq. 2-1)$$

where:

RD is the channel-to-flange device thermal resistance (K/W or °C/W)

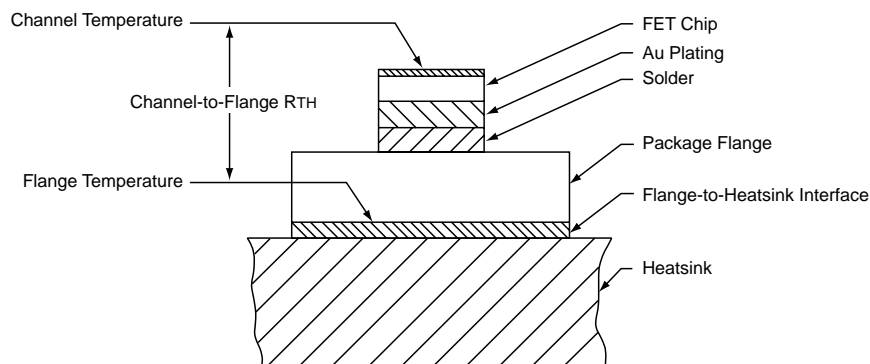
TCH is the channel temperature (K or °C)

TF is the case or flange temperature (K or °C)

PD is the power dissipated by the device, which is equal to the DC input power plus RF input power minus RF output power ( $P_D = V_{DS} \times I_{DS} + P_{IN} - P_{OUT}$ ) (W)

### 3-THERMAL CIRCUIT

Heat flow can be analyzed with a thermal circuit in the same way that current flow can be analyzed with an electrical circuit. In Fig. 2 the dissipated power (PD) is analogous to a current-source driver, temperatures are analogous to voltages, and each element in the thermal path has a thermal resistance (RTH) associated with it. The first element in the heat flow path is the channel-to-chip-bottom RTH (RC). The second element not shown in fig. 2 is the back side gold metalization (Au plated heat sink) of the chip Rth (RAu). The third element is the solder (interface chip-to-case) RTH (RS). The fourth



**Figure 1. Power FET Channel-to-Flange Thermal Resistance.**

element is the case or flange RTH (RF). The next element is the Rth associated with mounting the device on the heat sink (RI). The last element in the circuit shown is the heat sink-to-ambient RTH (RH).

The channel-to-flange RTH of the device alone (RD) which is given in the device data sheet consists of three practically constant RTH versus temperature, RAu, RS & RF, and the RTH of the GaAs chip, RC, which is a function of the temperature of the channel (TCH) and the temperature of the chip bottom (TCB):

$$RD = RF + RS + RAu + RC(TCH, TCB) \quad (Eq. 3-1)$$

**4-CASE OR FLANGE THERMAL RESISTANCE**

For the case of power GaAs devices, the chips are long and narrow and the thermal resistance of the flange can be approximated with the following formula:

$$RF = [LN (16 t / \pi W)] / (\pi \sigma_F N L) \quad (Eq. 4-1)$$

where:

- LN is the natural logarithm (or loge)
- RF is the case or flange thermal resistance (K/W)
- L is the length of the chip (cm)
- σF is the thermal conductivity of the flange material (W/cm.K)
- t is the flange thickness (cm)
- W is the width of the chip (cm)
- N is the number of chips used in the device

If these parameters cannot be obtained by the amplifier designer from the device supplier, the following assumption for power devices can be made:

$$RF = 0.3 RD \quad (Eq. 4-2)$$

where:

RD is the channel-to-flange device thermal resistance given in the data sheet.

**5-CHIP BACK SIDE METALIZATION AND SOLDER THERMAL RESISTANCE**

The thermal resistance of the chip back side metalization (RAu) is very low due to gold good thermal conductivity and the relative thin layer (2 to 30 um). This RTH can be disregarded for our purpose.

When the chips are correctly mounted to the flange (no voids underneath the chips), the interface chip-to-flange thermal resistance (RS) is low in comparison with the flange and chip RTH and can be ignored. It is about 2 to 3 % of the global device thermal resistance (RD).

If needed it can be approximated by assuming uniform heat flow through the interface chip-to-flange:

$$RS = t / (\sigma_s N L W) \quad (Eq. 5-1)$$

where:

- t is the solder thickness (cm)
- σs is the solder thermal conductivity (W/cm.K)
- N is the number of chips
- L is the chip length (cm)
- W is the chip width in (cm)

If these parameters cannot be obtained by the amplifier designer from the device supplier, the following assumption for power devices can be made:

$$RS = 0.025 RD \quad (Eq. 5-2)$$

The value of these parameters (RAu and RS) will be assumed to be negligible for the rest of this application note.

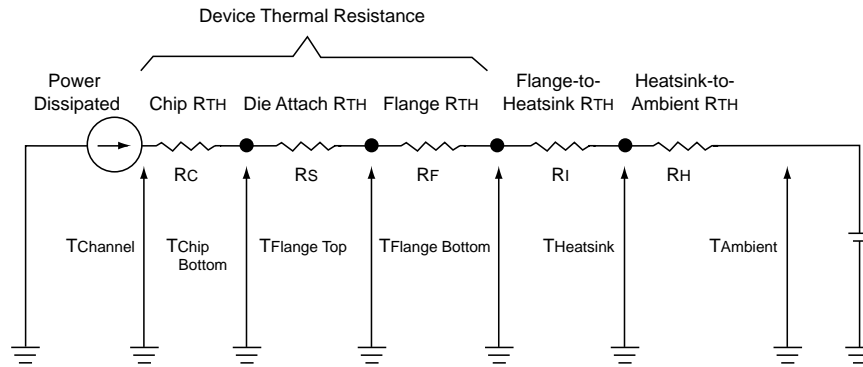


Figure 2. Thermal Circuit.

## 6-CHIP THERMAL RESISTANCE VERSUS TEMPERATURE

The thermal conductivity of the GaAs material can be expressed<sup>1,2</sup> by:

$$\sigma_{\text{GaAs}} = 0.44 [(T+273.2)/300]^{-1.25} \quad (\text{Eq. 6-1})$$

where:

$\sigma_{\text{GaAs}}$  is the GaAs substrate thermal conductivity at T (W/cm.K)

T is the temperature of the GaAs substrate (°C)

From this Eq. 6-1 and the Kirchoff's transformation the following formula can be derived (see appendix A):

$$R_{c2} = R_{c1} A/B \quad (\text{Eq. 6-2})$$

where:

$$A = [(T_{CH1} + 273.2)^{-0.25} - (T_{CB1} + 273.2)^{-0.25}] / (T_{CH1} - T_{CB1})$$

$$B = [(T_{CH2} + 273.2)^{-0.25} - (T_{CB2} + 273.2)^{-0.25}] / (T_{CH2} - T_{CB2})$$

**RC1** is the chip thermal resistance for a chip bottom temperature  $T_{CB1}$  and a channel temperature  $T_{CH1}$  (°C/W or K/W)

**RC2** is the chip thermal resistance for a chip bottom temperature  $T_{CB2}$  and a channel temperature  $T_{CH2}$  (°C/W or K/W)

**TCH1** and **TCH2** are the channel temperatures (°C)

**TCB1** and **TCB2** are the chip bottom temperatures (°C)

From the known thermal resistance ( $RC1$ ) of the chip for one set of temperatures ( $T_{CH1}$ ,  $T_{CB1}$ ), its thermal resistance ( $RC2$ ) can be calculated for any set of temperatures ( $T_{CH2}$ ,  $T_{CB2}$ ).

## 7-Methodology to Calculate Device Thermal Resistance versus Temperature from the Data Sheet Information (Fig. 3 shows the flow chart of this methodology)

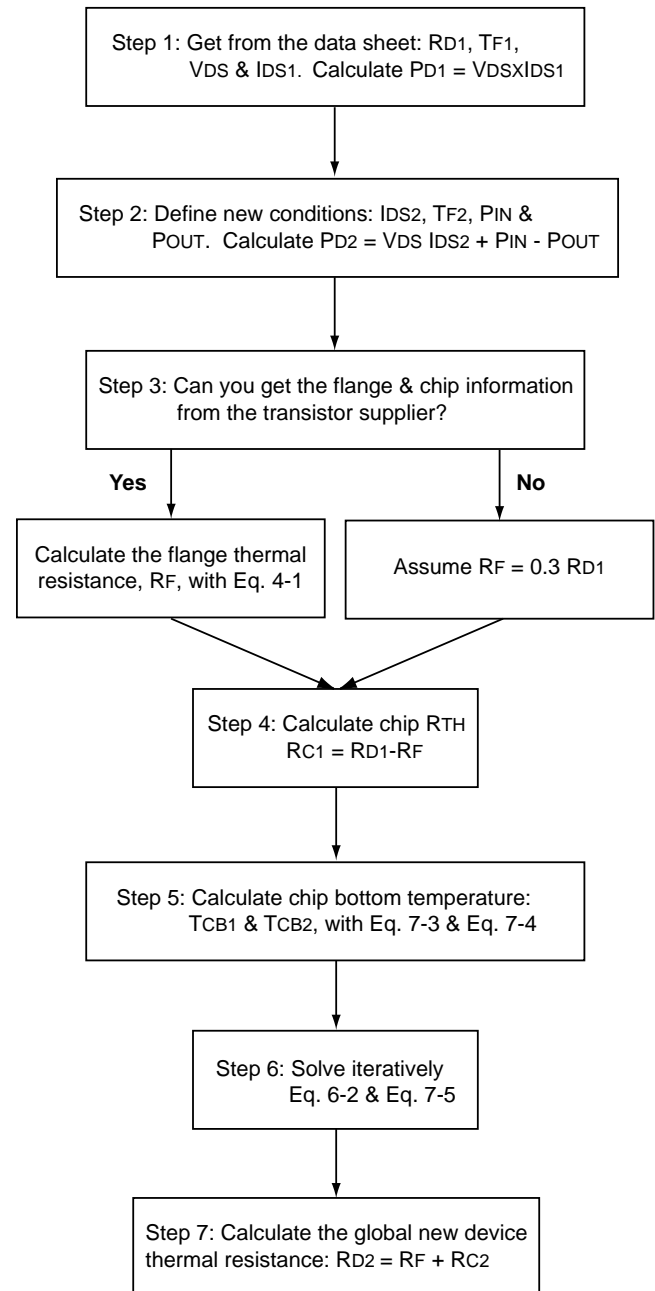


Figure 3. Thermal Resistance Calculation.

**Step 1: get RC1, TF1 and PD1 from the data sheet**

Get the value of the device thermal resistance (RD1) for a defined set of conditions from the data sheet. The measurement conditions are in general without RF. The drain-to-source voltage (VDS) and the drain current (IDS1) or the power dissipated (PD1=VDS IDS1) are given.

**Step 2: calculate PD2 from the new operating conditions**

The new conditions are defined by the application: IDS2, TF2, PIN & POUT.

The power dissipated is:

$$PD2=VDS IDS2+PIN-POUT \quad (Eq. 7-1)$$

where:

- VDS is the drain voltage (V)
- IDS2 is the drain current (A)
- PIN is the input power (W)
- POUT is the output power (W)

**Remark:**

VDS is assumed to be the same as the one defined in the data sheet because RD is a function of VDS.

**Step 3: calculate the flange thermal resistance (RF)**

From the device supplier or from measurement and literature get the flange thickness (t), and thermal conductivity (σF), the chip width (W) and length (L), the number of chips (N) used and use Eq. 4-1 to calculate the flange thermal resistance (RF).

If these parameters cannot be obtained from the device supplier or measured use Eq. 4-2:

**Step 4: calculate the chip thermal resistance for TF1 and TCH1**

$$RC1=RD1-RF \quad (Eq. 7-2)$$

**Step 5: calculate the chip bottom temperatures**

$$TCB1=TF1+RF PD1 \quad (Eq. 7-3)$$

$$TCB2=TF2+RF PD2 \quad (Eq. 7-4)$$

**Step 6: new chip thermal resistance (RC2) and channel temperature (TCH2)**

The following set of equations has to be solved:

$$RC2=RC1 A/B \quad (Eq. 6-2)$$

where:

$$A=[(TCH1+273.2)^{-0.25}-(TCB1+273.2)^{-0.25}] / (TCH1-TCB1)$$

$$B=[(TCH2+273.2)^{-0.25}-(TCB2+273.2)^{-0.25}] / (TCH2-TCB2)$$

and

$$TCH2=TCB2+RC2 PD2 \quad (Eq. 7-5)$$

It can be solved by using an iterative method. The n<sup>th</sup> approximation of the chip thermal resistance, RC2/n, and the channel temperature, TCH2/n, are obtained respectively from Eq. 6-2 and Eq. 7-5 in the n<sup>th</sup> step by using the previous approximation of RC2/n-1 and TCH2/n-1 obtained in the n-1<sup>th</sup> step.

The initial assumed values of RC2 and TCH2 for starting the first iteration, n=1, are respectively RC2/0=RC1 and TCH2/0=TCB2+RC1 PD2.

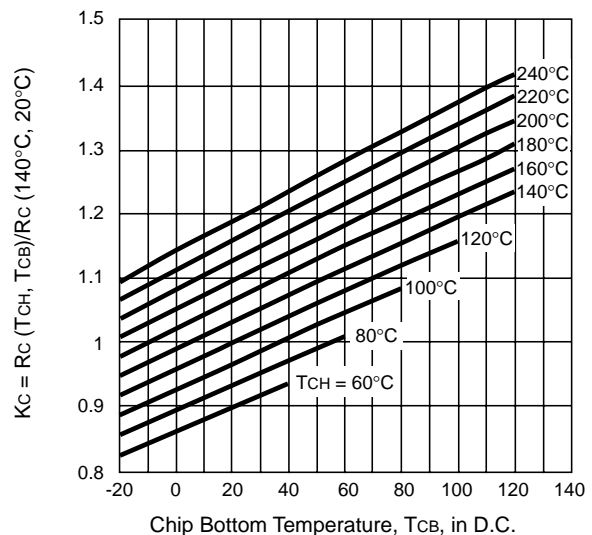
From the set of values, RC1, TCB1, TCH1, TCB2 and TCH2/n-1 and Eq. 6-2, calculate the nth approximation of RC2/n. Then calculate the nth approximation of TCH2/n from Eq. 7-5.

If the following double inequality is satisfied, -0.01<(RC2/n-RC2/n-1)/RC2/n-1<0.01 stop the iteration process, RC2=RC2/n and TCH2=TCH2/n

If this double inequality is not satisfied, then perform a n+1<sup>th</sup> iteration with the same process.

A small program may be written to solve this system of equations iteratively (see Appendix B) or, because this sequence converges to the solution rapidly (two to three iterations), a simple calculator with an exponential function may be used.

The graphical plot in Fig. 4 may also be used to calculate RC from Eq. 6-2. The plot represents the normalized chip thermal resistance, KC=RC/RC0, RC0 being the chip thermal resistance for TCHO=140°C and TCBO=20°C, versus TCH and TCB. To determine RC2 from the graphical plot Fig. 4, proceed as follows: first get KC1=RC1/RC0 for TCB1 and TCH1, then get KC2=RC2/RC0 for TCB2 and TCH2. The new thermal resistance value at TCB2 and TCH2 is given by the equation RC2=RC1 KC2/KC1.



**Figure 4. GaAS FET Chip RTH vs. Channel & Chip Bottom Temperature.**

**Step 7: Calculate RD2**

The new device Channel-to-flange thermal resistance at TCB2, TCH2 is:

$$RD2=RF+RC2 \quad (Eq. 7-6)$$

**Example 1****Step 1:**

The data sheet gives the following information:

RD1=1.04 K/W at TF1=25°C, VDS=10.0 V and IDS1=6.0 A  
The power dissipated is: PD1=10.0x6.0=60.0 W

**Step 2:**

This device is used for a reliability test at TF2=150°C with a power dissipated PD2= 60 W. Its thermal resistance needs to be known for these new operating conditions to calculate the device channel temperature.

**Step 3:**

The flange and chip parameters are unknown, we assumed in this case that:

$$RF=0.3 \quad RD1=0.3 \times 1.04=0.312 \text{ K/W}$$

**Step 4:**

The chip thermal resistance is: RC1=1.04-0.312=0.728 K/W

**Step 5:**

The chip bottom temperatures are:

$$TCB1=25+0.312 \times 60=43.7^\circ\text{C}$$

$$TCB2=150+0.312 \times 60=168.7^\circ\text{C}$$

**Step 6:****First iteration**

From Eq. 6-2 and RC1=0.728 K/W, TCB1=43.7°C, TCH1=25+1.04x60=87.4°C, TCB2=168.7°C, TCH2/0=168.7+0.728x60=212.4°C, calculate RC2/1: RC2/1=1.08 K/W, which corresponds to a difference of 48 % from the initial assumed value. A second iteration is necessary.

**Second iteration**

Perform a second iteration with TCH2/1=168.7+1.08x60=233.5°C, which gives: RC2/2=1.109 K/W which corresponds to a difference of 2.7 % from the assumed value RC2/1. A third iteration is necessary.

**Third iteration**

Perform a third iteration with TCH2/2=168.7+1.11x60=235.2°C, which gives: RC2/3=1.111 K/W which corresponds to a difference of 0.2 % from the assumed value RC2/2. A fourth iteration is not needed.

**Step 7:**

The new device thermal resistance is: RD2=1.111+0.312=1.423 K/W and TCH2=168.7+1.111x60=235.4°C

If the original value, RD1, were used it would introduce an error of -23.0°C for the channel temperature.

**Example 2****Step1:**

The data sheet gives the following information: RD=0.66 K/W at TF1=65°C, VDS=10.0 V and IDS1=12.0 A. The power dissipated is: PD1=10.0x12.0=120.0 W

**Step 2:**

This device is used at TF2=20°C and with PIN=3.0 W, POUT=60.0 W, IDS2=15 A, VDS=10.0 V. The power dissipated is: PD2=15.0x10.0+3.0-60.0=93.0 W

**Step 3:**

The flange is 0.178 cm thick and made of Cu/W-15 material with a thermal conductivity of 1.90 W/cm.K. Four chips are used and each chip is 0.42 cm long and 0.10 cm wide. From Eq.4-1, the flange thermal resistance can be calculated: RF=0.220 K/W

**Step 4:**

The chip thermal resistance is: RC1=0.660-0.220=0.440 K/W

**Step 5:**

The chip bottom temperatures are:

$$TCB1=65+0.220 \times 120=91.4^\circ\text{C}$$

$$TCB2=20+0.220 \times 93=40.5^\circ\text{C}$$

**Step 6:****First iteration**

From Eq. 6-2 and RC1=0.440 K/W, TCB1=91.4°C, TCH1=91.4+0.440x120=144.2°C, TCB2=40.5°C, TCH2/0=40.5+0.440x93=81.4°C, calculate RC2/1 : RC2/1=0.362 K/W, which corresponds to a difference of -18 % from the previous assumed value. A second iteration is needed.

**Second iteration**

Perform a second iteration with TCH2/1=40.5+0.362x93=74.2°C, which gives: RC2/2=0.357 K/W which corresponds to a difference of -1.4 %. A third iteration is needed.

**Third iteration**

Perform a third iteration with TCH2/2=40.5+0.357x93=73.7°C, which gives: RC2/3=0.357 K/W which corresponds to a difference of 0.1 %. A new iteration is not needed.

**Step 7:**

The new device thermal resistance is:  $RD_2=0.357+0.220=0.577$  K/W

If the original value,  $RD_1$ , were used it would introduce an error of  $7.5^\circ\text{C}$  for the channel temperature.

**Remarks:**

Sometimes the following formula is used to calculate device RTH versus channel temperature

$$RD_2=RD_1 (T_{CH2}/T_{CH1})^{-1.25}$$

where:

$T_{CH2}$  and  $T_{CH1}$  are the channel temperature in K

This is correct only if the  $TCB_1=T_{CH1}$  and  $TCB_2=T_{CH2}$ , in other terms if  $PD_1=PD_2=0$  W, which is rarely the case.

This formula doesn't take into account that the flange RTH which is constant versus temperature and has first to be subtracted from  $RD_1$  before applying any temperature correction.

**APPENDIX A**

**GaAs Chip Thermal Resistance versus Temperature**

**GaAs Material Thermal Conductivity versus Temperature**

The thermal conductivity of GaAs material is a function of the temperature and can be expressed by the following formula<sup>1,2</sup>:

$$\sigma_{GaAs}=A T^n \tag{Eq. A-1}$$

where:

$\sigma_{GaAs}$  is the GaAs material thermal conductivity at the temperature T (W/cm.K)

T is the GaAs material temperature (K)

$n=-1.25$

The dependence of  $\sigma_{GaAs}$  on the doping density is neglected because the regions where the material is doped are negligibly thick compared to the dimensions over which the heat is spread.

**Kirchhoff's Transformation**

The temperature dependence of the thermal conductivity of the GaAs chip can be taken into account by using the Kirchhoff's transformation. The method consists of solving the heat-flow equation, analytically, numerically, or empirically under the boundary conditions of usual interest. Then Kirchhoff's transformation immediately yields the nonlinear steady-state tem-

perature rise or thermal resistance of an uniform heat sink of any shape with no further approximations and negligible further effort.

At each point x of the conductor a fictitious linearized temperature  $\alpha(x)$  is associated with the actual temperature T(x) with the formula<sup>3</sup>:

$$\alpha(x)=T_0+\sigma_0^{-1} \int_{T_0}^T \sigma(T) dT \tag{Eq. A-2}$$

where  $\sigma_0=\sigma(T_0)$  is the thermal conductivity at  $T=T_0$ .

**Chip Thermal Resistance Versus Temperature**

Substituting the expression of  $\sigma$  from Eq. A-1 into Eq. A-2 and solving for the linearized channel temperature corresponding to chip bottom temperature  $TCB_1$  and channel temperature  $T_{CH1}$ :

$$\begin{aligned} \alpha l &= \alpha(T_{CB1}, T_{CH1}) = T_{CB1} + (A T_{CB1}^n)^{-1} \int_{T_{CB1}}^{T_{CH1}} A T^n dT \\ &= T_{CB1} + T_{CB1}^{-n} \left[ \frac{T^{n+1}}{(n+1)} \right]_{T_{CB1}}^{T_{CH1}} \\ \alpha l &= T_{CB1} + [(n+1) T_{CB1}^n]^{-1} (T_{CH1}^{n+1} - T_{CB1}^{n+1}) \end{aligned} \tag{Eq. A-3}$$

Using the definition of the thermal resistance given in Eq. 1-1 to solve for the linearized channel temperature we get:

$$\alpha l = T_{CB1} + R(\alpha l) PD1 \tag{Eq. A-4}$$

where  $R(\alpha l)$  is the linearized thermal resistance corresponding to the linearized channel temperature  $\alpha l$ . This is the value which the thermal resistance would have if the thermal conductivity of the GaAs material did not vary with temperature and was  $\sigma(T)=\sigma(T_{CB1})$ . We may express  $R(\alpha l)$  as:

$$R(\alpha l) = G/\sigma(T_{CB1}) = G T_{CB1}^{-n}/A \tag{Eq. A-5}$$

where  $\sigma(T_{CB1})$  is equal to the thermal conductivity of the material at a temperature of  $T_{CB1}$  [ $\sigma(T_{CB1})=A T_{CB1}^{-n}$ ], and G is a factor depending on the device geometry.

Substituting  $R(\alpha l)$  from Eq. A-5 into Eq. A-4:

$$\alpha l = T_{CB1} + PD1 G T_{CB1}^{-n}/A \text{ solving for PD1}$$

$$PD1 = (\alpha l - T_{CB1}) A T_{CB1}^n / G \tag{Eq. A-6}$$

We want to find the channel-to-chip-bottom thermal resistance at  $TCB_1$  and  $T_{CH1}$  defined as:

$$RC1 = (T_{CH1} - T_{CB1}) / PD1 \tag{Eq. A-7}$$

Substituting  $PD1$  from Eq. A-6 into Eq. A-7:

$$RC1 = G(T_{CH1} - T_{CB1}) / [A T_{CB1}^n (\alpha l - T_{CB1})] \tag{Eq. A-8}$$

Substituting the expression of  $\alpha 1$  from Eq. A-3 into Eq. A-8, we obtain after simplification:

$$RC1 = [G/A]^{(n+1)} (TCH1 - TCB1) / (TCB1^{n+1} - TCB2^{n+1}) \quad (Eq. A-9)$$

Similarly, for  $TCH = TCH2$  and  $TCB = TCB2$ ,  $RC2$  can be calculated:

$$RC2 = [G/A]^{(n+1)} (TCH2 - TCB2) / (TCH2^{n+1} - TCB2^{n+1}) \quad (Eq. A-10)$$

Dividing Eq. A-10 by Eq. A-9 and solving for  $RC2$  we obtain:

$$RC2 = RC1 \left[ \frac{(TCH1^{n+1} - TCB1^{n+1}) / (TCH1 - TCB1)}{(TCH2^{n+1} - TCB2^{n+1}) / (TCH2 - TCB2)} \right] \quad (Eq. A-11)$$

where:

**RC2:** chip channel-to-chip bottom thermal resistance at chip bottom temperature  $TCB2$  and at channel temperature  $TCH2$  (K/W)

**RC1:** chip channel-to-chip bottom thermal resistance at chip bottom temperature  $TCB1$  and at channel temperature  $TCH1$  (K/W)

**TCB1** and **TCB2:** are the chip bottom temperatures (K)

**TCH1** and **TCH2:** are the channel temperatures (K)

**T** in K = **T** in °C + 273.2

**n = -1.25**

## APPENDIX B

### HP48X or GX Calculator Program to Calculate GaAs Device Thermal Resistances versus Temperature

Here is an example of a program for a HP48X or GX calculator to calculate the thermal resistance of GaAs devices versus temperature when this parameter is already known for one operating point.

Begin by creating a directory for RTH, then get into that directory.

#### 1-Get subprograms

These following subprograms prompt the user to input a value for each of the following parameters:

RTH1 (device thermal resistance @ TF1 & TCH1 in K/W), TF1 (flange temperature in °C), TCH1 (channel temperature in °C), TF2 (flange temperature in °C), PD2 (power dissipated at TF2 & TCH2 in W), RF (flange thermal resistance in K/W) and n (n = -1.25).

```
<<"Key in RTH1 in K/W" " " INPUT OBJ -> 'RTH1' STO >>
ENTER 'GetRTH1' STO to put GetRTH in the stack and
store the program GetRTH1.
```

```
<<"Key in TF1 in D.C." " " INPUT OBJ -> 'TF1' STO >>
ENTER 'GetTF1' STO to put GetTF1 in the stack and store
the program GetTF1.
```

```
<<"Key in TCH1 in D.C." " " INPUT OBJ -> 'TCH1' STO >>
ENTER 'GetTCH1' STO to put GetTCH1 in the stack and
store the program GetTCH1.
```

```
<<"Key in TF2 in D.C." " " INPUT OBJ -> 'TF2' STO >>
ENTER 'GetTF2' STO to put GetTF2 in the stack and store
the program GetTF2.
```

```
<<"Key in PD2 in W" " " INPUT OBJ -> 'PD2' STO >>
ENTER 'GetPD2' STO to put GetPD2 in the stack and store
the program GetPD2.
```

```
<<"Key in n" " " INPUT OBJ -> 'Expo' STO >>
ENTER 'Getn' STO to put Getn in the stack and store the
program Getn.
```

#### 2-Compute subprograms

The compute subprograms handle the computational chores in the program.

```
<<'RTH1' RCL 'RF' RCL - 'RC1' STO 'RC1' RCL 'RC2' STO >>
ENTER 'CompRC1' STO to put CompRC1 in the stack and
store it.
```

```
<<'TCH1' RCL 'TF1' RCL - 'RTH1' RCL / 'PD1' STO >>
ENTER 'CompPD1' STO to put CompPD1 in the stack and
store it.
```

```
<<'RF' RCL 'PD1' RCL x 'TF1' RCL + 'TCB1' STO >>
ENTER 'CompTCB1' STO to put CompTCB1 in the stack and
store it.
```

```
<<'RF' RCL 'PD2' RCL x 'TF2' RCL + 'TCB2' STO >>
ENTER 'CompTCB2' STO to put CompTCB2 in the stack and
store it.
```

```
<<'TCB2' RCL 'PD2' RCL 'RC2' RCL x + 'TCH2' STO >>
ENTER 'CompTCH2' STO to put CompTCH2 in the stack and
store it.
```

```
<< 'Expo' RCL -> a b c << '((a+273.2)^(c+1))-
((b+273.2)^(c+1)) / (a-b)' EVAL -> NUM >> >>
ENTER 'CompAorB' STO to put CompAorB in the stack and
store it.
```

```
<< 'TCH1' RCL 'TCB1' RCL CompAorB 'TCH2' RCL
'TCB2' RCL CompAorB 'RC1' RCL -> a b c <<'axc/b'
EVAL -> NUM >> 'RC2' STO >>
```

```
ENTER 'CompRC2' STO to put CompRC2 in the stack and
store it.
```

#### 3-Label program

The final subprogram which adds a tag to the calculated  $RC2$  value.

```
<<"RTH2 in K/W=" -> TAG >>
```

```
ENTER 'Label' STO to put Label in the stack and store it
```

#### 4-Main program (five iterations are performed to calculate RC2)

```
<<GetRTH1 GetTF1 GetTCH1 GetTF2 GetPD2 GetPD2
GetRF Getn CompPD1 CompRC1 CompTCB1
```

**CompTCB2 1 5 START CompTCH2 CompRC2 NEXT  
'RC2' RCL 'RF' RCL + Label >>**

ENTER 'RCAL' STO to put Label in the stack and store it.

### 5-Running RCAL program

Run the RCAL program to find the Thermal Resistance of a device, RTH2, at TF2= 150°C and PD2= 60 W when its thermal resistance, RTH1, is known and is 1.04 K/W at TF1=25°C, and TCH1=87.4°C and knowing that its flange thermal resistance, RF, is 0.312 K/W.

Press RCAL

<b>Program Prompt or Display</b>	<b>Your Action</b>
Key in RTH1 (K/W)	1.04 ENTER
Key in TF1 (D.C.)	25 ENTER
Key in TCH1 (D.C.)	87.4 ENTER
Key in TF2 (D.C.)	150 ENTER
Key in PD2 (D.C.)	60 ENTER
Key in RF (K/W)	0.312 ENTER
Key in n	-1.25 ENTER
RTH2 in K/W= 1.423	

### References

1. Robert Anholt, "Electrical and Thermal Characterization of MESFETs, HEMTs, and HBTs" Artech House, Boston.London, chapter 4, page 62.
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