

## Low Cost, High Performance Receiver For Wireless Applications

### INTRODUCTION

With the increase in commercial applications of microwave and radio frequency (RF) equipment, designers have placed a greater demand on consistent performance and low price. The receiver front end described in this paper utilizes low-cost, off-the-shelf technology from NEC/California Eastern Labs to produce a circuit which can be used in many commercial designs.

The starting point for this circuit was the UPC2721GR MMIC down converter. This device includes a mixer with an internal local oscillator (LO) and an intermediate frequency (IF) buffer amplifier on a single MMIC chip. The internal LO is tuned using an external varactor diode. The UPC2721GR also allows the option of using an external oscillator.

In order to achieve an improved noise figure for the circuit, a low noise amplifier (LNA) was added at the RF input to the

down converter. The LNA was designed using a discrete low noise GaAs MESFET (NE76038) with a matching structure made using discrete components. The NE76038 is fabricated using ion implantation techniques to improve RF and DC performance, and features a recessed 0.3 micron gate and triple epitaxial technology. Typical noise figures of 1.8 dB can be obtained at 12 GHz, with 7.5 dB associated gain, even in the low cost plastic "38" package. The device is also available in ceramic packages and in chip form.

A low-pass filter was placed after the down converter to reduce the LO and RF power at the output, and an MMIC buffer amplifier (UPC2710T) was included at the end of the chain to increase the overall system gain. The UPC2710T features 33 dB typical gain up to 1500 MHz in an inexpensive six-pin minimold plastic package. A block diagram of the entire system is shown in Figure 1.

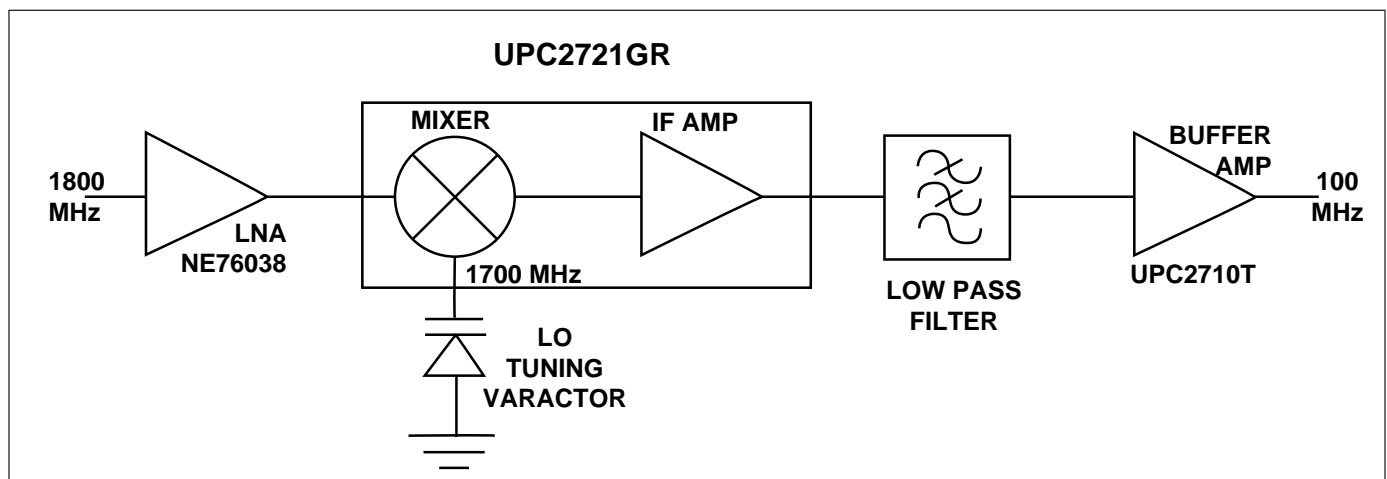


Figure 1. Block Diagram

Both the MMIC parts used in this design are manufactured using the NESAT III MMIC process developed by NEC. The process features include:

- A low-energy, boron-ion base implant which reduces base transit times
- A 0.6- $\mu\text{m}$  emitter line width which results in low base resistance and low parasitic capacitances.
- An arsenic ion-implanted buried layer and thin epitaxial layer to reduce collector resistance.
- Arsenic ion-implanted poly-silicon resistors on a thick SiO<sub>2</sub> layer to reduce parasitic capacitances of the on-chip resistors.
- PtSi/Ti/Pt/Au metallization and reactive ion etching to permit reliable production of 1- $\mu\text{m}$  electrode lines and gaps.
- A silicon nitride passivation layer for scratch and contamination protection.

These process features result in reliable and reproducible silicon MMICs with cutoff frequencies ( $f_T$ ) approaching 20 GHz.

**TARGET SPECIFICATIONS**

The design goal for this circuit was to produce a low-noise, high-gain receiver front-end. Operating frequency was to be 1800 MHz at the RF input, with a 1700 MHz LO resulting in a 100 MHz IF at the output. A further design goal was that the active parts used should be low cost: less than \$10 (based on 10K piece quantities). The design specs were as follows:

tested separately from the other components of the receiver. This was done so that the tuning elements could be optimized for minimum noise figure. The test circuit layout with the final values of the tuning elements is shown in Figure 2. 1800 MHz test results obtained from the final circuit were:

Small Signal Gain: 15.2 dB    Noise Figure: 0.6 dB  
 Input Return Loss: 5.2 dB    Output Return Loss: 3.5 dB

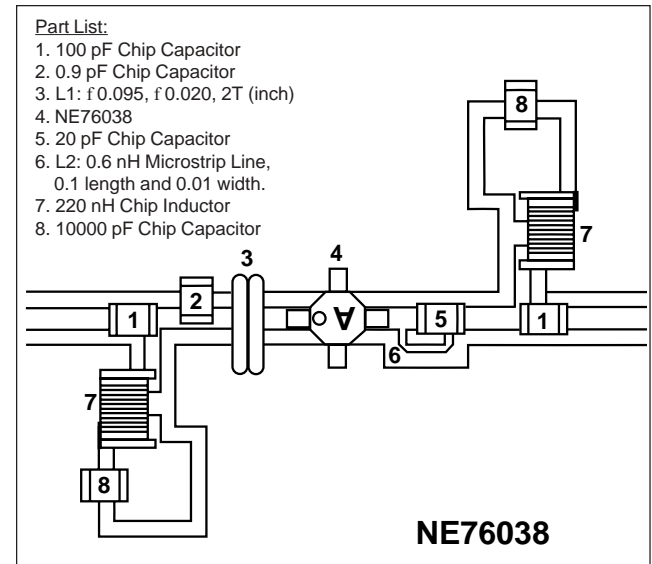


Figure 2. NE76038 LNA

Parameter	LN Amp	Mixer	Filter	IF Amp*	Overall
Gain (dB)	14	20	-6	32	60
Noise Figure (dB)	1	11	6	3.5	2.5
Saturation Power (dBm)	2	5	-	13	13
Input Return Loss (dB)	10	-	15	6	10
Output Return Loss (dB)	8	-	15	12	12
Cost (\$ @ 10K pc)**	\$2.10	\$2.00	-	\$1.70	\$5.70

\*LNA specs at 1800 MHz

\*\*Cost of active parts only

**DESIGN APPROACH**

Since the MMIC portions of this circuit are fixed in their performance, the design focused on the low noise amplifier. The NE76038 GaAs FET was chosen for its low noise figure, high reliability and low cost. The device was modeled using CAD (Touchstone) and the matching structure was optimized for a 100 MHz bandwidth centered at 1800 MHz. Discrete tuning elements were used with the goal of minimizing noise figure, while maintaining reasonable gain and return loss. The predicted circuit performance was 1.02 dB noise figure with 15.7 dB gain at 1800 MHz. Input and output return loss were predicted to be -9.9 dB and -8.3 dB respectively.

A test circuit for the low noise amplifier was assembled and

The next stage of the design was to test the low noise amplifier breadboard with the other components of the system. To accomplish this, separate test fixtures were built for each of the components in the chain. Test results on circuits for the down converter and the IF buffer amplifier were:

Down Converter: UPC2721GR  
 RF = 1800 MHz, LO = 1700 MHz  
 IF = 100 MHz  
 Conversion Gain: 19.5 dB

IF Amp: UPC2710T  
 Small Signal Gain: 33.5 dB  
 Input Return Loss: 9.8 dB  
 Output Return Loss: 14.0 dB



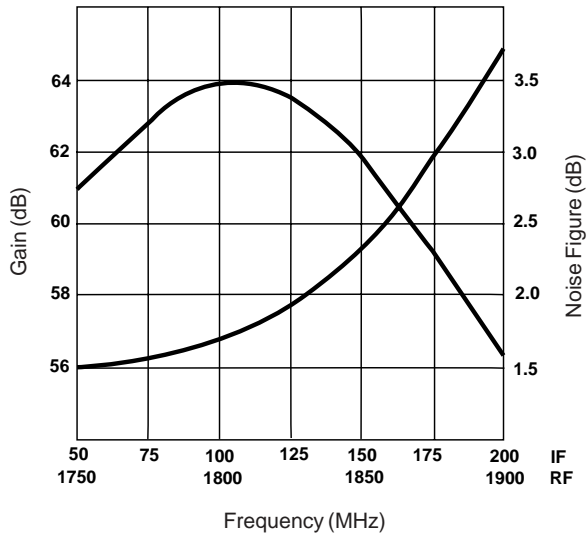


Figure 4. Gain & Noise Figure (Local Oscillator: 1700 MHz).

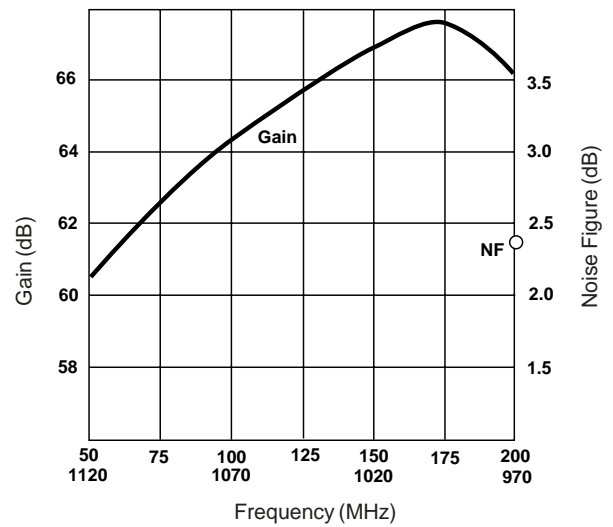


Figure 6. Modified Circuit Gain & Noise Figure (Local Oscillator: 1170 MHz)



Figure 5. NE76038 Low Noise Amp Layout.

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4590 Patrick Henry Drive, Santa Clara, CA 95054-1817  
 Telephone 408-988-3500 • FAX 408-988-0279 • Telex 34/6393  
 Internet: <http://WWW.CEL.COM>

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