

**AN-1001****RECOMMENDED HANDLING PROCEDURES FOR  
MICROWAVE TRANSISTOR AND MMIC CHIPS**

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**INTRODUCTION**

This document is provided to inform users of some of the handling precautions necessary and the assembly processes recommended in order to successfully use NEC microwave transistor and MMIC chips. Those who are unable to achieve satisfactory assembly results are encouraged to contact a CEL sales office for further assistance. CEL has a staff of experienced application engineers available to assist in resolving any problems that may be encountered.

**1.0 Electrostatic Discharge (ESD) Damage Precautions**

Microwave transistors are subject to degradation or destruction when exposed to electrostatic discharge (ESD). It is extremely important that the user be aware of this fact and take appropriate handling precautions to minimize or eliminate exposure of transistors to ESD. ESD exposure can result in reduced assembly yields and field reliability problems. The following steps are recommended to avoid ESD damage to transistor chips.

Chips are shipped with at least one packaging layer made of conductive material to shield from external sources of ESD. This conductive packaging should only be opened for removal of the chips at an ESD preventative work station. An ESD preventative work station should consist of, as a minimum, a conductive, grounded work surface and a grounded wrist strap with a current limiting resistor to be worn by the operator. Materials for constructing ESD preventative work stations are commercially available from several sources. CEL can provide a list of suppliers of ESD preventative materials to those who require it. CEL also recommends DOD-HDBK-263, "Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)" as an excellent reference source for establishment of an ESD prevention program. This handbook is available from the U.S. Department of Defense.

All assembly processing of transistor chips should be performed at ESD preventative work stations by operators wearing grounding straps. All assembly equipment used should be connected to electrical ground to avoid exposure of the chips to stray voltages.

Insulating materials which can readily take on a static electrical charge, such as styrofoam, plastic, and nylon, should be kept away from the vicinity of work stations. ESD preventative lab coats or smocks should be used to cover clothing made of synthetic materials worn by operators.

Work in process should be transported and stored in closed conductive containers. These containers should only be opened at ESD preventative work stations.

**2.0 Chip Storage**

It is recommended that all chips be stored in a clean, dry environment. Storage in a dry nitrogen (-50°C dew point) environment is preferable.

**3.0 Visual Inspection Criteria**

All transistor chips are 100% visually inspected to NEC's standard specifications. Copies of NEC's current visual inspection criteria are available from a CEL sales office.

**4.0 Chip Handling**

Transistor chips should always be handled in a clean environment, preferably under a laminar flow hood. Chips can be handled using a vacuum probe with a teflon or delrin tip, or with tweezers. Rubis model 5ASA tweezers are recommended for chip handling. Special caution must be exercised when han-

dling GaAs FET chips with tweezers. Ga-As is a very brittle material and edge chip-outs will occur if excessive pressure is used. GaAs FET chips should be gripped squarely and lightly with tweezers. See figure 1.

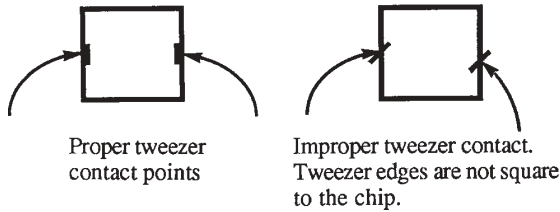


FIGURE 1

## 5.0 Die Attach

Bipolar transistor chips can be die attached by means of a collector with tweezers. Best results are achieved for GaAs FET chips by using the tweezers, as collets frequently cause edge damage. Eutectic die attach is recommended, although epoxy die attach is permissible for small signal or low noise transistors. The increased thermal resistance resulting from epoxy die attach must be taken into consideration if this method is used. Epoxy die attach cannot be recommended for any power transistors.

Eutectic die attach should be performed in a dry nitrogen atmosphere to avoid the formation of oxides. A suitable nitrogen environment can be achieved by directing a 200 liter per hour flow through a nozzle onto the surface to which the die will be attached. Forming gas composed of 95% nitrogen, and 5% hydrogen will reduce organic contaminants on the substrate surface and may be substituted for dry nitrogen. All NEC transistor chips have pure gold backside metallization to facilitate achieving good eutectic die attach. Die attachment is achieved by placing a eutectic preform in the proper location and then lightly "scrubbing" the chip on the preform. Silicon devices can also be eutectically attached to a gold plated substrate surface without the use of preforms when the gold plating thickness exceeds 100 microinches. If multiple components must be eutectically attached to a substrate, the transistor chips should be attached last to minimize the exposure time at temperature. The total chip exposure time should be limited to less than 5 minutes at 300°C, and less than one minute at 400°C. A typical exposure time of about 30 seconds can be expected for a skilled operator die attaching small signal transistor chips. The following listed eutectic alloys and die attach temperatures are recommended for the various types of NEC microwave transistor and MMIC chips.

- A. NPN Silicon Bipolar Chips and Silicon MMIC Chips:
  - a) AuSb (0.05% Sb) at 400°C ± 5°C.
  - b) AuSi (3% Si) at 400°C ± 5°C.
  - c) Au (100%) at 400°C ± 5°C.
  - d) AuSi (no preform) at 400°C ± 5°C.

- B. PNP Silicon Bipolar Chips
  - a) Au (100%) at 400°C ± 5°C.
  - b) AuSi (no preform) at 400°C ± 5°C.
- C. GaAs FET Chips and GaAs MMIC Chips:
  - a) AuSn (20% Sn) at 300°C ± 5°C.
  - b) AuGe (8% Ge) at 380°C ± 5°C.

Special handling procedures are required for power GaAs FET chips manufactured using NEC's plated heat sink (PHS) technology. These chips are large, very thin (60 ± 15 μm), and subject to the possibility of cracking due to the thermal shock encountered during the die attach process. This problem can be avoided by using a hot plate to preheat the chips and substrates to which they are being attached to an intermediate temperature for 2 minutes prior to placement on the die attach hot plate. After die attachment is completed, the reverse process is used for cool-down.

Example when using AuSn eutectic:

Ambient → 150°C → 300°C → 150°C → Ambient  
 Hot Plate Die Attach Hot Plate

Consult the appropriate CEL data sheet to determine if a power GaAs FET chip employs the PHS process.

## 5.1 Trouble Shooting the Die Attach Process

### A. Using Gold Alloy Preforms

The alloy elements and the percentage content in a preform will determine the melting temperature of the preform. Different alloys are available to meet particular electrical specifications or assembly requirements.

NEC/CEL uses 80% gold and 20% tin preforms with GaAs MESFETs and Hetero Junction (HJ) FETs. The working temperature should be well above the preform melting point so that full wetting can be assured. For this preform the recommended working temperature is 300 degrees C ± 5 degrees.

All preforms should be stored in a dry nitrogen atmosphere to prolong their life by keeping them free of contaminants & oxidation.

#### 1. Contaminated Preforms

Contaminated preforms can only be spotted during the die attachment process. A bad preform shows signs of a blackish, dull tint. Sample preforms should be tested before the die is scrubbed into the preform.

##### a) Testing

Place several preforms on a carrier. Use dry nitrogen or forming gas N<sub>2</sub>H<sub>2</sub> (95% / 5% respectively) to flow evenly over the hot plate at a rate of 200 liters per hour. A low power zoom microscope with 7 to 40

magnification will be sufficient to inspect the results. Place the carrier onto the hot plate and watch the preforms start to melt (5 to 10 seconds) and spread out the preforms with a tweezer.

Good Preforms: Will appear shiny and smooth and will flow smoothly over the carrier surface.

Bad preforms: Will appear dull and wrinkled. Bad preforms should be either discarded or cleaned. Buying preforms in small quantities and different lots assists in eliminating problems.

#### b) Cleaning

The cleaning method for preforms is the same as for cleaning a substrate (see section 7. 1). This can be time consuming and costly. It may be more cost effective to replace bad preforms.

#### c) Preform Sizes

Care should be exercised in choosing preforms of proper dimensions. Oversized preforms can increase costs and reduce die attach quality due to floating effect. Floating occurs when the preform is too large and results in poor thermal contact caused by the chip floating on a bubble of melted preform. It is best to order preforms that are slightly smaller than the chip being used and/or allow plenty of scrubbing space for excess preform material to flow. The recommended thickness for preforms is .001 inch.

### B. Die Attaching Procedure

1. Set preform in position where die is to rest.
2. Place die on same carrier to preheat.
3. Place carrier on hot plate.
4. Wait for preform to melt.
5. Scrub die onto preform - approximate time, 0 to 1 minute.
6. Remove carrier from hot plate and cool on metal block.

### C. Common Die Attach Problems

1. The Back of the Chip Wets 50% or Less
  - The back of the chip is contaminated.
  - The preforms are contaminated or oxidized.
  - There is not enough scrubbing action.
  - The process is performed in a non-clean environment.
  - Oxides are forming due to insufficient or improper flow of dry nitrogen or forning gas.
2. The Preform Does Not Wet Properly
  - The preform is contaminated or oxidized.
  - There is no forming gas or there is an incorrect mixture.
  - The substrate or carrier is contaminated.

## 6.0 Removal of Particulate from Chip Surface

Foreign particulate will occasionally be encountered on the surface of chips due to handling and exposure even when good procedures are used. In the case of power FET chips employing the PHS process, small pieces of the gold edge metallization will occasionally break off and be found on the surface of the chip or circuit substrate. This phenomenon is due to the process used to fabricate these chips which leaves a fragile edge area, but RF performance is not affected by this.

Such particulate can be removed after die attach by blowing them off of the chip and circuit surfaces with dry nitrogen. If this process is not feasible, a vacuum needle can be used to remove particulate.

### 6.1 Particulate Contamination Removal from Si and GaAs Chip Devices

At CEL we used the WASSCO TEL-K-150 Vacuum System for particulate contamination removal from Si and GaAs Chip Devices. Any equivalent system can also be used with satisfactory results. Below is the basic procedure used by CEL for particle contamination removal. This can be used as a guide when implementing a system other than that used by CEL.

- 1) Bend a Tel-1555 needle tip at the 2/3 length point at approximately a 45° angle for operator ease in particulate removal. See Figure 3.



FIGURE 3

- 2) Viewing the chip to be cleaned under a high power microscope, position the needle near and above the particulate contamination without touching the chip surface.
- 3) The operator then puts his finger over the vacuum hole in the probe and the particulate is sucked into the needle and carried away.
- 4) This is a somewhat delicate process and takes operator practice to develop the skill to remove contamination without scratching and damaging the chips. Approximately 1 hour per day for 1 week should be sufficient practice.



## B. Common Bonding Problems

1. Low Bond Strength Can Result From:
  - Contamination films on the wire, chip or substrate.
  - Insufficient bonding temperature.
  - Insufficient force on the bonding wedge.
  - Bond pad lifting.

- a) Contamination Films on the Wire, Chip or Substrate

Clean the effected surface by:

- Wire - soaking the spool of wire in alcohol.
- Substrates - cleaning in TCE, acetone, and alcohol for 15 minutes with ultrasonic.

- Chips - Bipolar or GaAs FET chips may be cleaned by plasma cleaning (ashing) or by use of alcohol based solvents. Bonding capillaries may also be cleaned, if they become contaminated, in ultrasonic using DI WATER only.

- b) Insufficient Temperature

Stage temperature can vary from ambient to 300 degrees C depending on the method used to die attach the chip onto the substrate or carrier. Epoxies are cured at approximately 150 degrees C. Preforms flow at 150 degrees C or above, depending on the per centage of gold used in eutectic mixture; the more gold, the higher the temperature. With 80% gold and 20% tin mixture (CEL's standard), the stage temperature is controlled to 240 degrees C, slightly below the melting temperature of the preform.

Tip temperature is completely dependent upon the bonding machine used. Most machines on the market today have the capability of temperatures ranging from ambient to 275°C. CEL controls the tip temperature at 180°C. The tip temperature varies inversely with the stage temperature to achieve a good bond.

For thermo-compression bonding, a capillary made of titanium carbide has proven to have a longer life when used at high temperatures.

- c) Insufficient Force on the Bonding Wedge Bonds that will not stick to the bonding pad may be caused by insufficient bonding force or by the wedge that is used.

\*CEL recommends the K & S "4200 Special" wedge made by Micro-Swiss. This wedge was designed to accommodate all of NEC's bond pad sizes.

## 2. Bond Pad Peeling

There are two major causes of this problem:

- a) Pad peels away cleanly from chip.

This effect is usually due to the use of ultrasonic bonding machines. The most obvious condition is when the wedge makes contact with the pad and causes immediate peeling. If the pad does not peel immediately, it may peel cleanly during bond pull. NEC/CEL does not recommend ultrasonic bonding for any of their devices.

- b) Cratering

This condition results in pad peeling with a cratering effect down into the chip surface. This is usually caused by too much bonding force.

### 8.0 Availability of Practice Chips:

Assembly practice chips are available from CEL at reduced cost for training of operators and development of assembly processes. It is recommended that these practice chips be used to develop operator skills prior to attempting circuit assembly with full specification devices. Contact your local sales office for more information.

#### NOTICE

These handling procedures are to be used only as guidelines. California Eastern Laboratories Inc. (CEL) assumes no liability for customer implementation of these procedures. CEL reserves the right to make changes in these handling procedures without notice.

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